

## Si4431 ISM TRANSCEIVER

### Features

- Frequency Range = 240–930 MHz
- Sensitivity = –118 dBm
- +13 dBm Max Output Power
  - Configurable –8 to +13 dBm
- Low Power Consumption
  - 18.5 mA receive
  - 28 mA @ +13 dBm transmit
- Data Rate = 1 to 128 kbps
- Power Supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-on-radio
- Auto-frequency calibration (AFC)
- Antenna diversity and TR switch control
- Configurable packet structure
- Preamble detector
- TX and RX 64 byte FIFOs
- Low battery detector
- Temperature sensor and 8-bit ADC
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-Pin QFN package
- FSK, GFSK, and OOK modulation
- Low BOM
- Power-on-reset (POR)

### Applications

- Remote control
- Home security & alarm
- Telemetry
- Personal data logging
- Toy control
- Tire pressure monitoring
- Wireless PC peripherals
- Remote meter reading
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Tag readers

### Description

Silicon Laboratories' Si4431 highly integrated, single chip wireless ISM transceiver is part of the EZRadioPRO™ family. The EZRadioPRO family includes a complete line of transmitters, receivers, and transceivers allowing the RF system designer to choose the optimal wireless part for their application.

The Si4431 offers advanced radio features including continuous frequency coverage from 240–930 MHz. The Si4431's high level of integration offers reduced BOM cost while simplifying the overall system design. The extremely low receive sensitivity (–118 dBm) coupled with industry leading +20 dBm output power ensures extended range and improved link performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance.

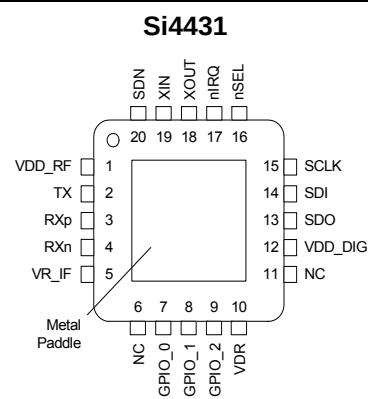
Additional system features such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, automatic packet handling, and preamble detection reduce overall current consumption and allow the use of lower-cost system MCUs. An integrated temperature sensor, general purpose ADC, power-on-reset (POR), and GPIOs further reduce overall system cost and size.

The Si4431's digital receive architecture features a high-performance ADC and DSP based modem which performs demodulation, filtering, and packet handling for increased flexibility and performance. This digital architecture simplifies system design while allowing for the use of lower-end MCUs. The direct digital transmit modulation and automatic PA power ramping ensure precise transmit modulation and reduced spectral spreading ensuring compliance with FCC and ETSI regulations.



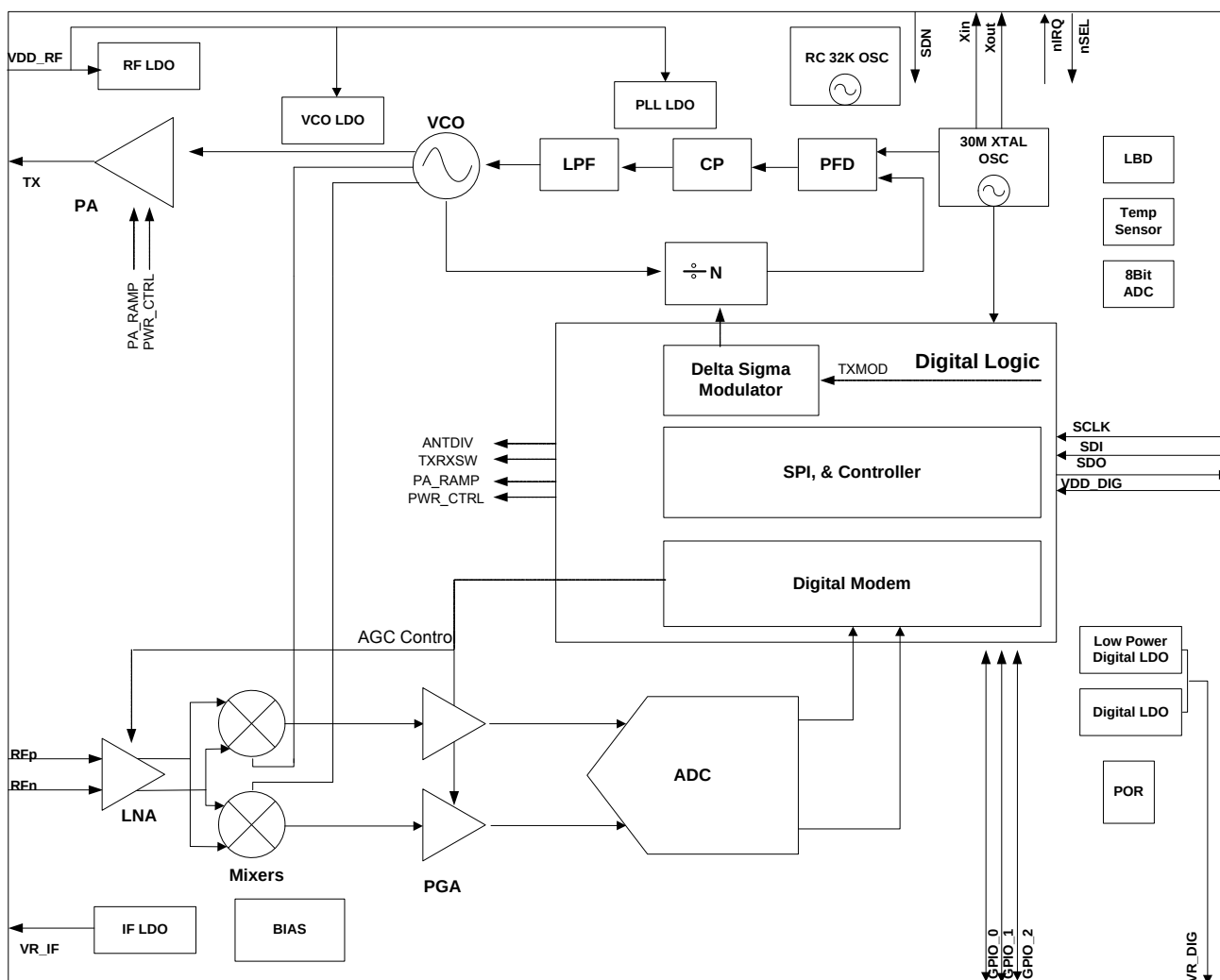
**Ordering Information:**  
See page 156.

### Pin Assignments



Patents pending

## Functional Block Diagram



# TABLE OF CONTENTS

| <b><u>Section</u></b>                             | <b><u>Page</u></b> |
|---------------------------------------------------|--------------------|
| <b>1. Electrical Specifications</b>               | <b>8</b>           |
| 1.1. Definition of Test Conditions                | 15                 |
| <b>2. Functional Description</b>                  | <b>16</b>          |
| 2.1. Operating Modes                              | 18                 |
| <b>3. Controller Interface</b>                    | <b>19</b>          |
| 3.1. Serial Peripheral Interface (SPI)            | 19                 |
| 3.2. Operating Mode Control                       | 21                 |
| 3.3. Interrupts                                   | 24                 |
| 3.4. Device Code                                  | 24                 |
| 3.5. System Timing                                | 25                 |
| 3.6. Frequency Control                            | 27                 |
| <b>4. Modulation Options</b>                      | <b>34</b>          |
| 4.1. Modulation Type                              | 34                 |
| 4.2. Modulation Data Source                       | 35                 |
| 4.3. FIFO Mode                                    | 35                 |
| 4.4. Direct Mode                                  | 35                 |
| 4.5. PN9 Mode                                     | 36                 |
| 4.6. Synchronous vs. Asynchronous                 | 36                 |
| <b>5. Internal Functional Blocks</b>              | <b>38</b>          |
| 5.1. RX LNA                                       | 38                 |
| 5.2. RX I-Q Mixer                                 | 38                 |
| 5.3. Programmable Gain Amplifier                  | 38                 |
| 5.4. ADC                                          | 38                 |
| 5.5. Digital Modem                                | 38                 |
| 5.6. Synthesizer                                  | 39                 |
| 5.7. Power Amplifier                              | 40                 |
| 5.8. Crystal Oscillator                           | 41                 |
| 5.9. Regulators                                   | 41                 |
| <b>6. Data Handling and Packet Handler</b>        | <b>42</b>          |
| 6.1. RX and TX FIFOs                              | 42                 |
| 6.2. Packet Configuration                         | 43                 |
| 6.3. Packet Handler TX Mode                       | 44                 |
| 6.4. Packet Handler RX Mode                       | 44                 |
| 6.5. Data Whitening, Manchester Encoding, and CRC | 47                 |
| 6.6. Preamble Detector                            | 47                 |
| 6.7. Preamble Length                              | 47                 |
| 6.8. Invalid Preamble Detector                    | 48                 |
| 6.9. TX Retransmission and Auto TX                | 48                 |
| <b>7. RX Modem Configuration</b>                  | <b>49</b>          |

|                                                      |            |
|------------------------------------------------------|------------|
| 7.1. Modem Settings for FSK and GFSK .....           | 49         |
| 7.2. Modem Settings for OOK .....                    | 52         |
| <b>8. Auxiliary Functions .....</b>                  | <b>55</b>  |
| 8.1. Smart Reset .....                               | 55         |
| 8.2. Microcontroller Clock .....                     | 56         |
| 8.3. General Purpose ADC .....                       | 57         |
| 8.4. Temperature Sensor .....                        | 60         |
| 8.5. Low Battery Detector .....                      | 62         |
| 8.6. Wake-Up Timer .....                             | 63         |
| 8.7. Low Duty Cycle Mode .....                       | 65         |
| 8.8. GPIO Configuration .....                        | 66         |
| 8.9. Antenna-Diversity .....                         | 67         |
| 8.10. RSSI and Clear Channel Assessment .....        | 68         |
| <b>9. Reference Design .....</b>                     | <b>69</b>  |
| <b>10. Measurement Results .....</b>                 | <b>73</b>  |
| <b>11. Application Notes .....</b>                   | <b>78</b>  |
| 11.1. Crystal Selection .....                        | 78         |
| 11.2. Layout Practice .....                          | 78         |
| 11.3. Matching Network Design .....                  | 79         |
| <b>12. Reference Material .....</b>                  | <b>81</b>  |
| 12.1. Complete Register Table and Descriptions ..... | 81         |
| <b>13. Pin Descriptions: Si4431 .....</b>            | <b>155</b> |
| <b>14. Ordering Information .....</b>                | <b>156</b> |
| <b>15. Package Information .....</b>                 | <b>157</b> |
| <b>Contact Information .....</b>                     | <b>158</b> |

## LIST OF FIGURES

|                                                                                     |    |
|-------------------------------------------------------------------------------------|----|
| Figure 1. Si4431 RX/TX Direct-Tie Application Example .....                         | 17 |
| Figure 2. SPI Timing.....                                                           | 19 |
| Figure 3. SPI Timing—READ Mode .....                                                | 20 |
| Figure 4. SPI Timing—Burst Write Mode .....                                         | 20 |
| Figure 5. SPI Timing—Burst Read Mode .....                                          | 20 |
| Figure 6. State Machine Diagram.....                                                | 21 |
| Figure 7. TX Timing.....                                                            | 25 |
| Figure 8. RX Timing .....                                                           | 26 |
| Figure 9. Frequency Deviation .....                                                 | 30 |
| Figure 10. Sensitivity at 1% PER vs. Carrier Frequency Offset .....                 | 31 |
| Figure 11. FSK vs GFSK Spectrums.....                                               | 34 |
| Figure 12. Direct Synchronous Mode Example .....                                    | 36 |
| Figure 13. Direct Asynchronous Mode Example .....                                   | 36 |
| Figure 14. FIFO Mode Example .....                                                  | 37 |
| Figure 15. PLL Synthesizer Block Diagram.....                                       | 39 |
| Figure 16. FIFO Thresholds .....                                                    | 42 |
| Figure 17. Packet Structure.....                                                    | 43 |
| Figure 18. Multiple Packets in TX Packet Handler .....                              | 44 |
| Figure 19. Required RX Packet Structure with Packet Handler Disabled .....          | 44 |
| Figure 20. Multiple Packets in RX Packet Handler.....                               | 44 |
| Figure 21. Multiple Packets in RX with CRC or Header Error .....                    | 45 |
| Figure 22. Operation of Data Whitening, Manchester Encoding, and CRC .....          | 47 |
| Figure 23. POR Glitch Parameters.....                                               | 55 |
| Figure 24. General Purpose ADC Architecture .....                                   | 57 |
| Figure 25. ADC Differential Input Example—Bridge Sensor .....                       | 58 |
| Figure 26. ADC Differential Input Offset for Sensor Offset Coarse Compensation..... | 59 |
| Figure 27. Temperature Ranges using ADC8 .....                                      | 61 |
| Figure 28. WUT Interrupt and WUT Operation.....                                     | 64 |
| Figure 29. Low Duty Cycle Mode .....                                                | 65 |
| Figure 30. RSSI Value vs. Input Power.....                                          | 68 |
| Figure 31. Split RF I/Os with Separated TX and RX Connectors—Schematic .....        | 69 |
| Figure 32. Split RF I/Os with Separated TX and RX Connectors—Top .....              | 71 |
| Figure 33. Split RF I/Os with Separated TX and RX Connectors—Top Silkscreen .....   | 71 |
| Figure 34. Split RF I/Os with Separated TX and RX Connectors—Bottom.....            | 72 |
| Figure 35. Sensitivity vs. Data Rate .....                                          | 73 |
| Figure 36. Receiver Selectivity.....                                                | 74 |
| Figure 37. TX Modulation (40 kbps, 20 kHz Deviation).....                           | 75 |
| Figure 38. TX Unmodulated Spectrum (917 MHz).....                                   | 75 |
| Figure 39. TX Modulated Spectrum (917 MHz, 40 kbps, 20 kHz Deviation, GFSK).....    | 76 |
| Figure 40. Synthesizer Settling Time for 1 MHz Jump Settled within 10 kHz .....     | 76 |
| Figure 41. Synthesizer Phase Noise (VCOCURR = 11) .....                             | 77 |
| Figure 42. RX LNA Matching.....                                                     | 79 |
| Figure 43. TX Matching and Filtering for Different Bands .....                      | 79 |

Figure 44. QFN-20 Package Dimensions..... 157

Figure 45. QFN-20 Landing Pattern Dimensions ..... 157



## LIST OF TABLES

|                                                                                           |     |
|-------------------------------------------------------------------------------------------|-----|
| Table 1. DC Characteristics .....                                                         | 8   |
| Table 2. Synthesizer AC Electrical Characteristics <sup>1</sup> .....                     | 9   |
| Table 3. Receiver AC Electrical Characteristics <sup>1</sup> .....                        | 10  |
| Table 4. Transmitter AC Electrical Characteristics <sup>1</sup> .....                     | 11  |
| Table 5. Auxiliary Block Specifications <sup>1</sup> .....                                | 12  |
| Table 6. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ) .....                 | 13  |
| Table 7. GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2) .....                           | 13  |
| Table 8. Absolute Maximum Ratings .....                                                   | 14  |
| Table 9. Operating Modes .....                                                            | 18  |
| Table 10. Serial Interface Timing Parameters .....                                        | 19  |
| Table 11. Operating Modes .....                                                           | 21  |
| Table 12. Frequency Band Selection .....                                                  | 28  |
| Table 13. RX Packet Handler Configuration .....                                           | 45  |
| Table 14. Packet Handler Registers .....                                                  | 46  |
| Table 15. Minimum Receiver Settling Time .....                                            | 48  |
| Table 16. RX Modem Configurations for FSK and GFSK .....                                  | 49  |
| Table 17. Filter Bandwidth Parameters .....                                               | 51  |
| Table 18. Channel Filter Bandwidth Settings .....                                         | 52  |
| Table 19. ndec[2:0] Settings .....                                                        | 53  |
| Table 20. RX Modem Configuration for OOK with Manchester Disabled .....                   | 54  |
| Table 21. RX Modem Configuration for OOK with Manchester Enabled .....                    | 54  |
| Table 22. POR Parameters .....                                                            | 55  |
| Table 23. Temperature Sensor Range .....                                                  | 60  |
| Table 24. Antenna Diversity Control .....                                                 | 67  |
| Table 25. Split RF I/Os Bill of Materials .....                                           | 70  |
| Table 26. Recommended Crystal Parameters .....                                            | 78  |
| Table 27. RX Matching for Different Bands .....                                           | 79  |
| Table 28. Register Descriptions .....                                                     | 81  |
| Table 29. Interrupt or Status 1 Bit Set/Clear Description .....                           | 86  |
| Table 30. When are Individual Status Bits Set/Cleared if not Enabled as Interrupts? ..... | 86  |
| Table 31. Interrupt or Status 2 Bit Set/Clear Description .....                           | 88  |
| Table 32. Detailed Description of Status Registers when not Enabled as Interrupts .....   | 88  |
| Table 33. Internal Analog Signals Available on the Analog Test Bus .....                  | 128 |
| Table 34. Internal Digital Signals Available on the Digital Test Bus .....                | 129 |

## 1. Electrical Specifications

Table 1. DC Characteristics

| Parameter                                                                                                                                                                           | Symbol           | Conditions                                                                                                               | Min | Typ  | Max | Units   |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------|
| Supply Voltage Range                                                                                                                                                                | $V_{dd}$         |                                                                                                                          | 1.8 | 3.0  | 3.6 | V       |
| Power Saving Modes                                                                                                                                                                  | $I_{Shutdown}$   | RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF <sup>2</sup>                                  | —   | 10   | TBD | nA      |
|                                                                                                                                                                                     | $I_{Standby}$    | Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF <sup>1</sup> | —   | 400  | —   | nA      |
|                                                                                                                                                                                     | $I_{Sleep}$      | RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF <sup>1</sup>  | —   | 800  | —   | nA      |
|                                                                                                                                                                                     | $I_{Sensor-LBD}$ | Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>             | —   | 1    | —   | $\mu$ A |
|                                                                                                                                                                                     | $I_{Sensor-TS}$  | Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF <sup>2</sup>               | —   | 1    | —   | $\mu$ A |
|                                                                                                                                                                                     | $I_{Ready}$      | Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled <sup>1</sup>  | —   | 600  | —   | $\mu$ A |
| TUNE Mode Current                                                                                                                                                                   | $I_{Tune}$       | Synthesizer and regulators enabled                                                                                       | —   | 9.5  | —   | mA      |
| RX Mode Current                                                                                                                                                                     | $I_{RX}$         |                                                                                                                          | —   | 18.5 | —   | mA      |
| TX Mode Current                                                                                                                                                                     | $I_{TX\_+13}$    | txpow[2:0] = 11 (+13 dBm), VDD = 3.3 V                                                                                   | —   | 28   | —   | mA      |
|                                                                                                                                                                                     | $I_{TX\_+1}$     | txpow[2:0] = 00 (+1 dBm), VDD = 3.3 V                                                                                    | —   | 18   | —   | mA      |
| <b>Notes:</b> <ol style="list-style-type: none"> <li>1. All specification guaranteed by production test unless otherwise noted.</li> <li>2. Guaranteed by qualification.</li> </ol> |                  |                                                                                                                          |     |      |     |         |

Table 2. Synthesizer AC Electrical Characteristics<sup>1</sup>

| Parameter                                     | Symbol                           | Conditions                                                                                    | Min | Typ    | Max | Units              |
|-----------------------------------------------|----------------------------------|-----------------------------------------------------------------------------------------------|-----|--------|-----|--------------------|
| Synthesizer Frequency Range                   | F <sub>SYNTH-LB</sub>            | Low Band                                                                                      | 240 | —      | 480 | MHz                |
|                                               | F <sub>SYNTH-HB</sub>            | High Band                                                                                     | 480 | —      | 930 | MHz                |
| Synthesizer Frequency Resolution <sup>2</sup> | F <sub>RES-LB</sub>              | Low Band                                                                                      | —   | 156.25 | —   | Hz                 |
|                                               | F <sub>RES-HB</sub>              | High Band                                                                                     | —   | 312.5  | —   | Hz                 |
| Reference Frequency                           | f <sub>REF</sub>                 | f <sub>crystal</sub> / 3                                                                      | —   | 10     | —   | MHz                |
| Reference Frequency Input Level <sup>2</sup>  | f <sub>REF_LV</sub>              | When using reference frequency instead of crystal. Measured peak-to-peak (V <sub>PP</sub> )   | 0.7 | —      | 1.6 | V                  |
| Synthesizer Settling Time <sup>2</sup>        | t <sub>LOCK</sub>                | Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration | —   | 200    | —   | μs                 |
| Residual FM <sup>2</sup>                      | ΔF <sub>RMS</sub>                | Integrated over ±250 kHz bandwidth (500 Hz lower bound of integration)                        | —   | 2      | 4   | kHz <sub>RMS</sub> |
| Phase Noise <sup>2</sup>                      | L <sub>φ</sub> (f <sub>M</sub> ) | ΔF = 10 kHz                                                                                   | —   | –80    | —   | dBc/Hz             |
|                                               |                                  | ΔF = 100 kHz                                                                                  | —   | –90    | —   | dBc/Hz             |
|                                               |                                  | ΔF = 1 MHz                                                                                    | —   | –115   | —   | dBc/Hz             |
|                                               |                                  | ΔF = 10 MHz                                                                                   | —   | –130   | —   | dBc/Hz             |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 3. Receiver AC Electrical Characteristics<sup>1</sup>

| Parameter                                                                                           | Symbol                | Conditions                                                                                                                                                          | Min | Typ     | Max | Units    |
|-----------------------------------------------------------------------------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|-----|----------|
| RX Frequency Range                                                                                  | F <sub>SYNTH-LB</sub> | Low Band                                                                                                                                                            | 240 | —       | 480 | MHz      |
|                                                                                                     | F <sub>SYNTH-HB</sub> | High Band                                                                                                                                                           | 480 | —       | 930 | MHz      |
| RX Sensitivity                                                                                      | P <sub>RX_2</sub>     | (BER < 0.1%)<br>(2 kbps, GFSK, BT = 0.5,<br>$\Delta f = \pm 5$ kHz) <sup>2</sup>                                                                                    | —   | –118    | —   | dBm      |
|                                                                                                     | P <sub>RX_40</sub>    | (BER < 0.1%)<br>(40 kbps, GFSK, BT = 0.5,<br>$\Delta f = \pm 20$ kHz) <sup>2</sup>                                                                                  | —   | –107    | —   | dBm      |
|                                                                                                     | P <sub>RX_100</sub>   | (BER < 0.1%)<br>(100 kbps, GFSK, BT = 0.5,<br>$\Delta f = \pm 50$ kHz) <sup>2</sup>                                                                                 | —   | –103    | —   | dBm      |
|                                                                                                     | P <sub>RX_125</sub>   | (BER < 0.1%)<br>(125 kbps, GFSK, BT = 0.5,<br>$\Delta f = \pm 62.5$ kHz) <sup>1</sup>                                                                               | —   | –101    | —   | dBm      |
|                                                                                                     | P <sub>RX_OOK</sub>   | (BER < 0.1%)<br>(4.8 kbps, 350 kHz BW, OOK) <sup>2</sup>                                                                                                            | —   | –110    | —   | dBm      |
|                                                                                                     |                       | (BER < 0.1%)<br>(40 kbps, 400 kHz BW, OOK) <sup>1</sup>                                                                                                             | —   | –102    | —   | dBm      |
| RX Bandwidth <sup>2</sup>                                                                           | BW                    |                                                                                                                                                                     | 2.6 | —       | 620 | kHz      |
| Residual BER Performance <sup>2</sup>                                                               | P <sub>RX_RES</sub>   | Up to +5 dBm Input Level                                                                                                                                            | —   | 0       | 0.1 | ppm      |
| Input Intercept Point,<br>3 <sup>rd</sup> Order <sup>2</sup>                                        | IIP3 <sub>RX</sub>    | f <sub>1</sub> = 915 MHz, f <sub>2</sub> = 915 MHz,<br>P <sub>1</sub> = P <sub>2</sub> = –40 dBm                                                                    | —   | –20     | —   | dBm      |
| LNA Input Impedance <sup>2</sup><br>(Unmatched, measured<br>differentially across RX<br>input pins) | R <sub>IN-RX</sub>    | 915 MHz                                                                                                                                                             | —   | 40–55j  | —   | $\Omega$ |
|                                                                                                     |                       | 868 MHz                                                                                                                                                             | —   | 44–58j  | —   |          |
|                                                                                                     |                       | 433 MHz                                                                                                                                                             | —   | 79–110j | —   |          |
|                                                                                                     |                       | 315 MHz                                                                                                                                                             | —   | 96–134j | —   |          |
| RSSI Resolution                                                                                     | RES <sub>RSSI</sub>   |                                                                                                                                                                     | —   | ±0.5    | —   | dB       |
| ±1-Ch Offset Selectivity <sup>2</sup><br>(BER < 0.1%)                                               | C/I <sub>1-CH</sub>   | Desired Ref Signal 3 dB above sensitivity.<br>Interferer and desired modulated with<br>40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5,<br>channel spacing = 150 kHz | —   | –31     | —   | dB       |
| ±2-Ch Offset Selectivity <sup>2</sup><br>(BER < 0.1%)                                               | C/I <sub>2-CH</sub>   |                                                                                                                                                                     | —   | –35     | —   | dB       |
| ≥ ±3-Ch Offset Selectivity <sup>2</sup><br>(BER < 0.1%)                                             | C/I <sub>3-CH</sub>   |                                                                                                                                                                     | —   | –40     | —   | dB       |
| Blocking at 1 MHz <sup>2</sup>                                                                      | 1M <sub>BLOCK</sub>   | Desired Ref Signal 3 dB above sensitivity.<br>Interferer and desired modulated with<br>40 kbps $\Delta F = 20$ kHz GFSK with BT = 0.5                               | —   | –52     | —   | dB       |
| Blocking at 4 MHz <sup>2</sup>                                                                      | 4M <sub>BLOCK</sub>   |                                                                                                                                                                     | —   | –56     | —   | dB       |
| Blocking at 8 MHz <sup>2</sup>                                                                      | 8M <sub>BLOCK</sub>   |                                                                                                                                                                     | —   | –63     | —   | dB       |
| Image Rejection <sup>2</sup>                                                                        | Im <sub>REJ</sub>     | IF=937 kHz                                                                                                                                                          | —   | –30     | —   | dB       |
| Spurious Emissions <sup>2</sup>                                                                     | P <sub>OB_RX1</sub>   | Measured at RX pins<br>(LO feed through)                                                                                                                            | —   | —       | –54 | dBm      |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 4. Transmitter AC Electrical Characteristics<sup>1</sup>

| Parameter                                                 | Symbol                | Conditions                                                                                                                         | Min    | Typ   | Max  | Units |
|-----------------------------------------------------------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------|--------|-------|------|-------|
| TX Frequency Range <sup>1</sup>                           | F <sub>SYNTH-LB</sub> | Low Band                                                                                                                           | 240    | —     | 480  | MHz   |
|                                                           | F <sub>SYNTH-HB</sub> | High Band                                                                                                                          | 480    | —     | 930  |       |
| FSK Modulation Data Rate <sup>2</sup>                     | DR <sub>FSK</sub>     |                                                                                                                                    | 1      | —     | 128  | kbps  |
| OOK Modulation Data Rate <sup>2</sup>                     | DR <sub>OOK</sub>     |                                                                                                                                    | 1.2    | —     | 40   | kbps  |
| Modulation Deviation <sup>1</sup>                         | Δf                    | Production tests maximum limit of 320 kHz                                                                                          | ±0.625 |       | ±320 | kHz   |
| Modulation Deviation Resolution                           | Δf <sub>RES</sub>     |                                                                                                                                    | —      | 0.625 | —    | kHz   |
| Output Power Range <sup>1</sup>                           | P <sub>TX</sub>       | Power control by txpow[2:0] Register<br>Production test at txpow[2:0] = 111<br>Tested at 915 MHz                                   | −8     | —     | +13  | dBm   |
| TX RF Output Steps <sup>2</sup>                           | ΔP <sub>RF_OUT</sub>  | controlled by txpow[2:0] Register                                                                                                  | —      | 3     | —    | dB    |
| TX RF Output Level Variation vs. Voltage <sup>2</sup>     | ΔP <sub>RF_V</sub>    | Measured from VDD=3.6 V to VDD=1.8 V                                                                                               | —      | 2     | —    | dB    |
| TX RF Output Level <sup>2</sup> Variation vs. Temperature | ΔP <sub>RF_TEMP</sub> | −40 to +85 °C                                                                                                                      | —      | 2     | —    | dB    |
| TX RF Output Level Variation vs. Frequency <sup>2</sup>   | ΔP <sub>RF_FREQ</sub> | Measured across any one frequency band                                                                                             | —      | 1     | —    | dB    |
| Transmit Modulation Filtering <sup>2</sup>                | B*T                   | Gaussian Filtering Bandwidth Time Product                                                                                          | —      | 0.5   | —    |       |
| Spurious Emissions <sup>2</sup>                           | P <sub>OB-TX1</sub>   | P <sub>OUT</sub> = 11 dBm,<br>Frequencies <1 GHz                                                                                   | —      | —     | −54  | dBm   |
|                                                           | P <sub>OB-TX2</sub>   | 1–12.75 GHz, excluding harmonics                                                                                                   | —      | —     | −54  | dBm   |
| Harmonics <sup>2</sup>                                    | P <sub>2HARM</sub>    | Using Reference Design TX Matching Network and Filter with Max Output Power (+13 dBm). Harmonics reduce linearly with output power | —      | —     | −42  | dBm   |
|                                                           | P <sub>3HARM</sub>    |                                                                                                                                    | —      | —     | −42  | dBm   |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

**Table 5. Auxiliary Block Specifications<sup>1</sup>**

| Parameter                                                      | Symbol               | Conditions                                                                        | Min     | Typ  | Max | Units |
|----------------------------------------------------------------|----------------------|-----------------------------------------------------------------------------------|---------|------|-----|-------|
| Temperature Sensor Accuracy <sup>2</sup>                       | TS <sub>A</sub>      | When calibrated using temp sensor offset register                                 | —       | 0.5  | —   | °C    |
| Temperature Sensor Sensitivity <sup>2</sup>                    | TS <sub>S</sub>      |                                                                                   | —       | 5    | —   | mV/°C |
| Low Battery Detector Resolution <sup>2</sup>                   | LBD <sub>RES</sub>   |                                                                                   | —       | 50   | —   | mV    |
| Low Battery Detector Conversion Time <sup>2</sup>              | LBD <sub>CT</sub>    |                                                                                   | —       | 250  | —   | μs    |
| Microcontroller Clock Output Frequency                         | MC                   | Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz | 32.768K | —    | 30M | Hz    |
| General Purpose ADC Accuracy <sup>2</sup>                      | ADC <sub>ENB</sub>   |                                                                                   | —       | 8    | —   | bit   |
| General Purpose ADC Resolution <sup>2</sup>                    | ADC <sub>RES</sub>   |                                                                                   | —       | 4    | —   | mV    |
| Temp Sensor & General Purpose ADC Conversion Time <sup>2</sup> | ADC <sub>CT</sub>    |                                                                                   | —       | 305  | —   | μsec  |
| 30 MHz XTAL Start-Up time                                      | t <sub>30M</sub>     | With the recommended XTAL parameters shown in Table 26 on page 78                 | —       | 1    | —   | ms    |
| 30 MHz XTAL Cap Resolution <sup>2</sup>                        | 30M <sub>RES</sub>   | See "5.8. Crystal Oscillator" on page 41 for total load capacitance calculation   | —       | 97   | —   | fF    |
| 32 kHz XTAL Start-Up Time <sup>2</sup>                         | t <sub>32k</sub>     |                                                                                   | —       | 6    | —   | sec   |
| 32 kHz XTAL Accuracy <sup>2</sup>                              | 32K <sub>RES</sub>   |                                                                                   | —       | 100  | —   | ppm   |
| 32 kHz RC OSC Accuracy <sup>2</sup>                            | 32KRC <sub>RES</sub> |                                                                                   | —       | 2500 | —   | ppm   |
| POR Reset Time                                                 | t <sub>POR</sub>     |                                                                                   | —       | 16   | —   | ms    |
| Software Reset Time <sup>2</sup>                               | t <sub>soft</sub>    |                                                                                   | —       | 100  | —   | μs    |

**Notes:**

1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification.

Table 6. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)

| Parameter                       | Symbol     | Conditions                                                | Min            | Typ | Max | Units |
|---------------------------------|------------|-----------------------------------------------------------|----------------|-----|-----|-------|
| Rise Time                       | $T_{RISE}$ | $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$ , $C_L = 5$ pF | —              | —   | 8   | ns    |
| Fall Time                       | $T_{FALL}$ | $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$ , $C_L = 5$ pF | —              | —   | 8   | ns    |
| Input Capacitance               | $C_{IN}$   |                                                           | —              | —   | 1   | pF    |
| Logic High Level Input Voltage  | $V_{IH}$   |                                                           | $V_{DD} - 0.6$ | —   | —   | V     |
| Logic Low Level Input Voltage   | $V_{IL}$   |                                                           |                | —   | 0.6 | V     |
| Input Current                   | $I_{IN}$   | $0 < V_{IN} < V_{DD}$                                     | –100           | —   | 100 | nA    |
| Logic High Level Output Voltage | $V_{OH}$   | $I_{OH} < 1$ mA source, $V_{DD} = 1.8$ V                  | $V_{DD} - 0.6$ | —   | —   | V     |
| Logic Low Level Output Voltage  | $V_{OL}$   | $I_{OL} < 1$ mA sink, $V_{DD} = 1.8$ V                    | —              | —   | 0.6 | V     |

**Note:** All specification guaranteed by production test unless otherwise noted.

Table 7. GPIO Specifications (GPIO\_0, GPIO\_1, and GPIO\_2)

| Parameter                            | Symbol       | Conditions                                                                 | Min            | Typ | Max | Units |
|--------------------------------------|--------------|----------------------------------------------------------------------------|----------------|-----|-----|-------|
| Rise Time                            | $T_{RISE}$   | $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$ ,<br>$C_L = 10$ pF, DRV<1:0>=HH | —              | —   | 8   | ns    |
| Fall Time                            | $T_{FALL}$   | $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$ ,<br>$C_L = 10$ pF, DRV<1:0>=HH | —              | —   | 8   | ns    |
| Input Capacitance                    | $C_{IN}$     |                                                                            | —              | —   | 1   | pF    |
| Logic High Level Input Voltage       | $V_{IH}$     |                                                                            | $V_{DD} - 0.6$ | —   |     | V     |
| Logic Low Level Input Voltage        | $V_{IL}$     |                                                                            | —              | —   | 0.6 | V     |
| Input Current                        | $I_{IN}$     | $0 < V_{IN} < V_{DD}$                                                      | –100           | —   | 100 | nA    |
| Input Current If Pullup is Activated | $I_{INP}$    | $V_{IL} = 0$ V                                                             | 5              | —   | 25  | μA    |
| Maximum Output Current               | $I_{OmaxLL}$ | DRV<1:0>=LL                                                                | 0.1            | 0.5 | 0.8 | mA    |
|                                      | $I_{OmaxLH}$ | DRV<1:0>=LH                                                                | 0.9            | 2.3 | 3.5 | mA    |
|                                      | $I_{OmaxHL}$ | DRV<1:0>=HL                                                                | 1.5            | 3.1 | 4.8 | mA    |
|                                      | $I_{OmaxHH}$ | DRV<1:0>=HH                                                                | 1.8            | 3.6 | 5.4 | mA    |
| Logic High Level Output Voltage      | $V_{OH}$     | $I_{OH} < I_{Omax}$ source,<br>$V_{DD} = 1.8$ V                            | $V_{DD} - 0.6$ | —   | —   | V     |
| Logic Low Level Output Voltage       | $V_{OL}$     | $I_{OL} < I_{Omax}$ sink,<br>$V_{DD} = 1.8$ V                              | —              | —   | 0.6 | V     |

**Note:** All specification guaranteed by production test unless otherwise noted.

**Table 8. Absolute Maximum Ratings**

| Parameter                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Value                | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|------|
| $V_{DD}$ to GND                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | -0.3, +3.6           | V    |
| $V_{DD}$ to GND on TX Output Pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | -0.3, +8.0           | V    |
| Voltage on Digital Control Inputs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | -0.3, $V_{DD} + 0.3$ | V    |
| Voltage on Analog Inputs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | -0.3, $V_{DD} + 0.3$ | V    |
| RX Input Power                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | +10                  | dBm  |
| Operating Ambient Temperature Range $T_A$                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | -40 to +85           | °C   |
| Thermal Impedance $\theta_{JA}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 30                   | °C/W |
| Junction Temperature $T_J$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | +125                 | °C   |
| Storage Temperature Range $T_{STG}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | -55 to +125          | °C   |
| <b>Note:</b> Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.<br>Power Amplifier may be damaged if switched on without proper load or termination connected. |                      |      |

## 1.1. Definition of Test Conditions

### Production Test Conditions:

$T_A = +25\text{ }^{\circ}\text{C}$

$V_{DD} = +3.3\text{ VDC}$

External reference signal (XIN) = 1.0 V<sub>PP</sub> at 30 MHz, centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4431 (not the RF module)

### Extreme Test Conditions:

$T_A = -40\text{ to }+85\text{ }^{\circ}\text{C}$

$V_{DD} = +1.8\text{ to }+3.6\text{ VDC}$

External reference signal (XIN) = 0.7 to 1.6 V<sub>PP</sub> at 30 MHz centered around 0.8 VDC

Production test schematic (unless noted otherwise)

All RF input and output levels referred to the pins of the Si4431 (not the RF module)

### Test Notes:

All electrical parameters with Min/Max values are guaranteed by one (or more) of the following test methods. Electrical parameters shown with only Typical values are not guaranteed.

- Guaranteed by design and/or simulation but not tested.
- Guaranteed by Engineering Qualification testing at Extreme Test Conditions.
- Guaranteed by 100% Production Test Screening at Production Test Conditions.

## 2. Functional Description

The Si4431 is a 100% CMOS ISM wireless transceiver with continuous frequency tuning over the complete 240–930 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption makes the Si4431 an ideal solution for battery powered applications.

The Si4431 operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion, image-reject mixer to downconvert the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance  $\Delta\Sigma$  ADC allowing filtering, demodulation, slicing, error correction, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is then output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and  $\Delta\Sigma$  Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 240–930 MHz. The transmit FSK data is modulated directly into the  $\Delta\Sigma$  data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

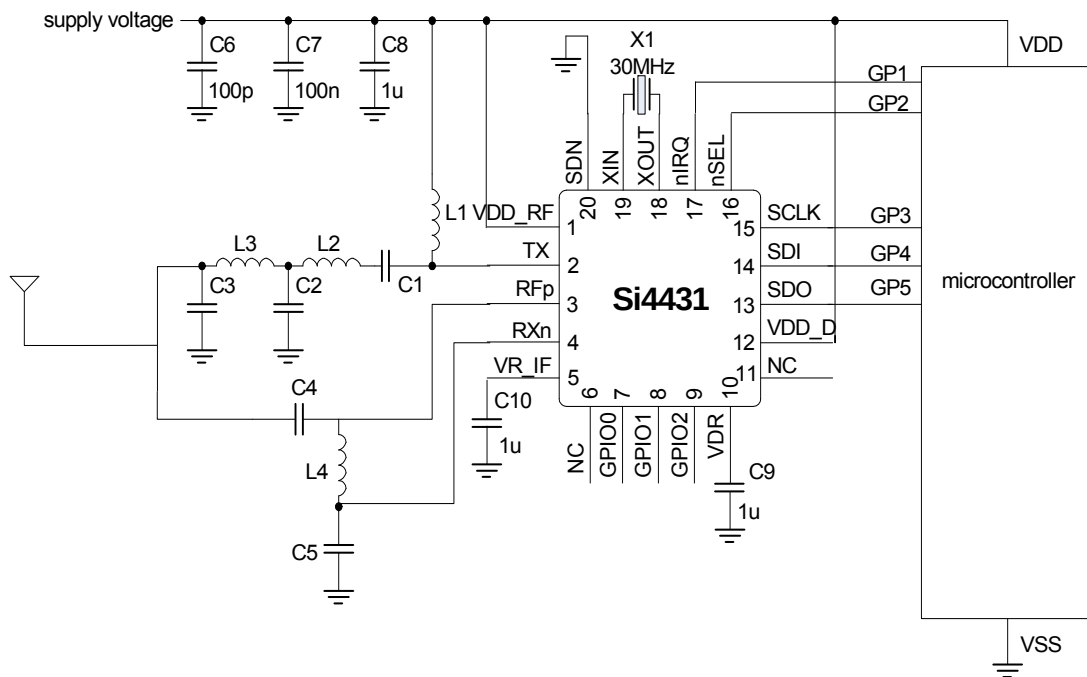
The PA output power can be configured between –8 and +13 dBm in 3 dB steps. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si4431 supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Antenna diversity is completely integrated into the Si4431 and can improve the system link budget by 8–10 dB, resulting in substantial range increases depending on the environmental conditions.

The Si4431 is designed to work with a microcontroller, crystal, and a few passives to create a very low cost system as shown Figure 1. Voltage regulators are integrated on-chip which allow for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general purpose I/Os are available for use to tailor towards the needs of the system. A more complete list of the available GPIO functions is shown in "8. Auxiliary Functions" on page 55 but just to name a few, microcontroller clock output, Antenna Diversity, POR, and specific interrupts. A limited number of passive components are needed to match the LNA and PA.

The application shown in Figure 1 is designed for a system with an TX/RX direct-tie configuration without the use of a TX/RX switch. Most lower power applications will use this configuration. A direct-tie reference design is available from Silicon Laboratories applications support.

For applications seeking improved performance in the presence of multipath fading antenna diversity can be used. Antenna diversity includes a switch to select the optimal antenna between a pair of antennas for improved performance. The Antenna Diversity Control Algorithm is completely integrated into the chip. A complete Antenna Diversity reference design is available from Silicon Laboratories applications support.

An application example with a separate RX and TX antenna is shown in Figure 31, "Split RF I/Os with Separated TX and RX Connectors—Schematic," on page 69. This example is used for testing of the TX and RX paths in a lab environment and shows, conceptually, the matching of the TX and RX antennas.



Programmable load capacitors for X1 are integrated.  
 R1, L1-L5 and C1-C4 values depend on frequency band,  
 antenna impedance, output power and supply voltage range.

**Figure 1. Si4431 RX/TX Direct-Tie Application Example**

## 2.1. Operating Modes

The Si4431 provides several modes of operation which can be used to optimize the power consumption of the device application. Depending upon the system communication protocol, the optimal trade-off between the radio wake time and power consumption can be achieved.

Table 9 summarizes the modes of operation of the Si4431. In general, any given mode of operation may be classified as an Active mode or a Power Saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI in order to optimize the average current consumption. An “X” in any cell means that, in the given mode of operation, that block can be independently programmed to be either ON or OFF, without noticeably affecting the current consumption. The SPI circuit block includes the SPI interface and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator, and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor, general purpose ADC, and low-battery detector.

**Table 9. Operating Modes**

| Mode Name                | Circuit Blocks                  |     |            |     |             |     |     |     |                  |
|--------------------------|---------------------------------|-----|------------|-----|-------------|-----|-----|-----|------------------|
|                          | Digital LDO                     | SPI | 32 kHz OSC | AUX | 30 MHz XTAL | PLL | PA  | RX  | I <sub>VDD</sub> |
| Shutdown                 | OFF (Register contents lost)    | OFF | OFF        | OFF | OFF         | OFF | OFF | OFF | 10 nA            |
| Standby                  | ON (Register contents retained) | ON  | OFF        | OFF | OFF         | OFF | OFF | OFF | 400 nA           |
| Sleep                    |                                 | ON  | ON         | X   | OFF         | OFF | OFF | OFF | 800 nA           |
| Sensor                   |                                 | ON  | X          | ON  | OFF         | OFF | OFF | OFF | 1 μA             |
| Ready                    |                                 | ON  | X          | X   | ON          | OFF | OFF | OFF | 600 μA           |
| Tuning                   |                                 | ON  | X          | X   | ON          | ON  | OFF | OFF | 9.5 mA           |
| Transmit                 |                                 | ON  | X          | X   | ON          | ON  | ON  | OFF | 28 mA*           |
| Receive                  |                                 | ON  | X          | X   | ON          | ON  | OFF | ON  | 18.5 mA          |
| *Note: 28 mA at +13 dBm. |                                 |     |            |     |             |     |     |     |                  |

### 3. Controller Interface

#### 3.1. Serial Peripheral Interface (SPI)

The Si4431 communicates with the host MCU over a 3 wire SPI interface: SCLK, SDI, and nSEL. The host MCU can also read data from internal registers on the SDO output pin. A SPI transaction is a 16-bit sequence which consists of a Read-Write ( $\overline{R}/W$ ) select bit, followed by a 7-bit address field (ADDR), and an 8-bit data field (DATA), as demonstrated in Figure 2. The 7-bit address field supports reading from or writing to one of the 128, 8-bit control registers. The  $\overline{R}/W$  select bit determines whether the SPI transaction is a write or read transaction. If  $\overline{R}/W = 1$ , it signifies a WRITE transaction, while  $\overline{R}/W = 0$  signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4431 every eight clock cycles. The timing parameters for the SPI interface are shown in Table 10. The SCLK rate is flexible with a maximum rate of 10 MHz.

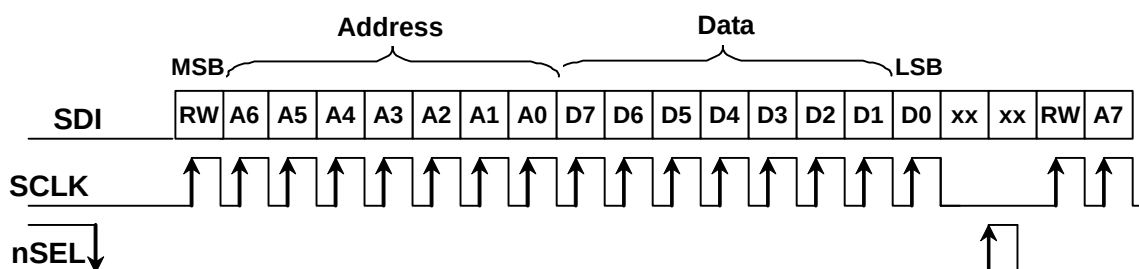


Figure 2. SPI Timing

Table 10. Serial Interface Timing Parameters

| Symbol   | Parameter              | Min (nsec) | Diagram |
|----------|------------------------|------------|---------|
| $t_{CH}$ | Clock high time        | 40         |         |
| $t_{CL}$ | Clock low time         | 40         |         |
| $t_{DS}$ | Data setup time        | 20         |         |
| $t_{DH}$ | Data hold time         | 20         |         |
| $t_{DD}$ | Output data delay time | 20         |         |
| $t_{EN}$ | Output enable time     | 20         |         |
| $t_{DE}$ | Output disable time    | 50         |         |
| $t_{SS}$ | Select setup time      | 20         |         |
| $t_{SH}$ | Select hold time       | 50         |         |
| $t_{SW}$ | Select high period     | 80         |         |

To read back data from the Si4431, the  $\overline{R}/W$  bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored when  $\overline{R}/W = 0$ . The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 3. After the READ function is completed the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pullup.

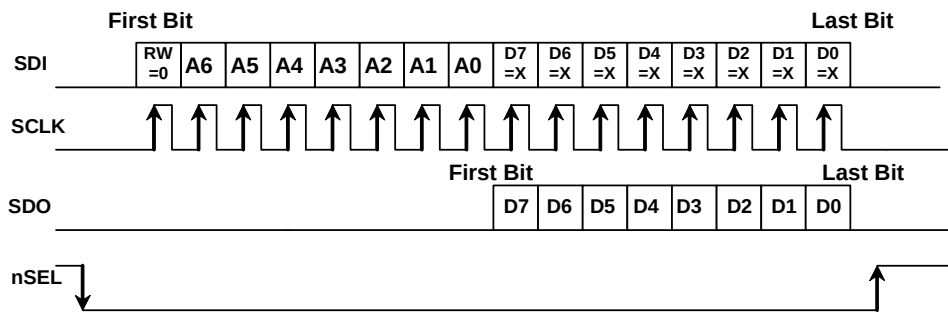


Figure 3. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode which will allow for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An SPI burst write transaction is demonstrated in Figure 4 and burst read in Figure 3. As long as nSEL is held low, input data will be latched into the Si4431 every eight SCLK cycles. A burst read transaction is also demonstrated in Figure 5.

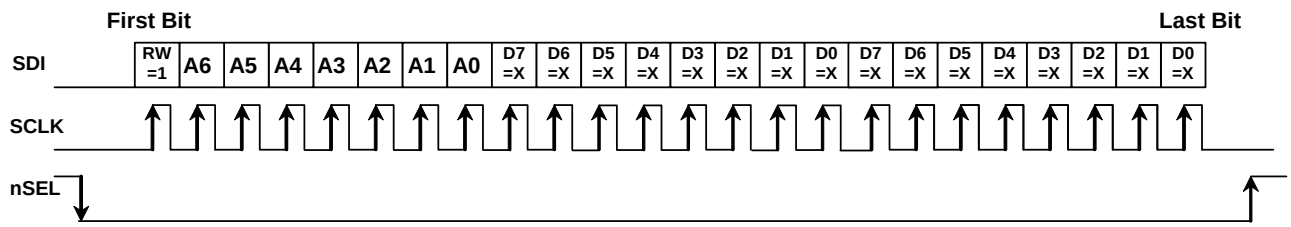


Figure 4. SPI Timing—Burst Write Mode

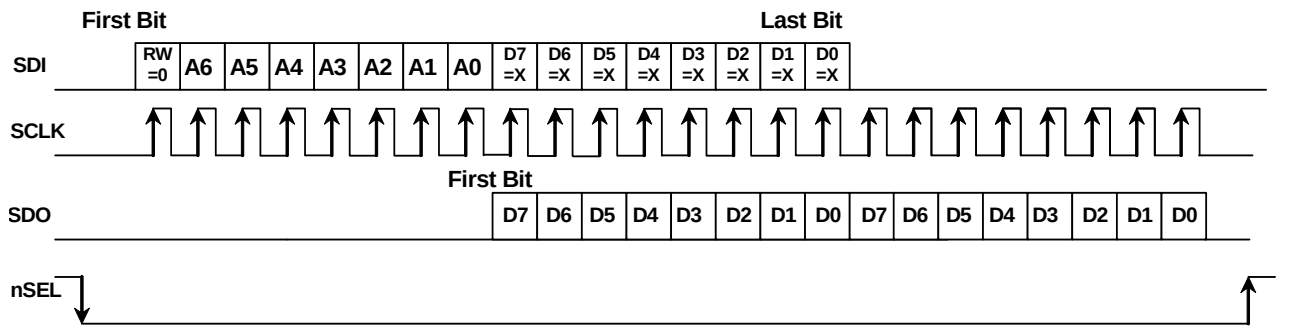


Figure 5. SPI Timing—Burst Read Mode

### 3.2. Operating Mode Control

There are four primary states in the Si4431 radio state machine: SHUTDOWN, IDLE, TX, and RX (see Figure 6). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. "Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The TX and RX state may be reached automatically from any of the IDLE states by setting the txon/rxon bits in "Register 07h. Operating Mode and Function Control 1". Table 11 shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode.

The output of the LPLDO is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR\_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, and SPI and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.

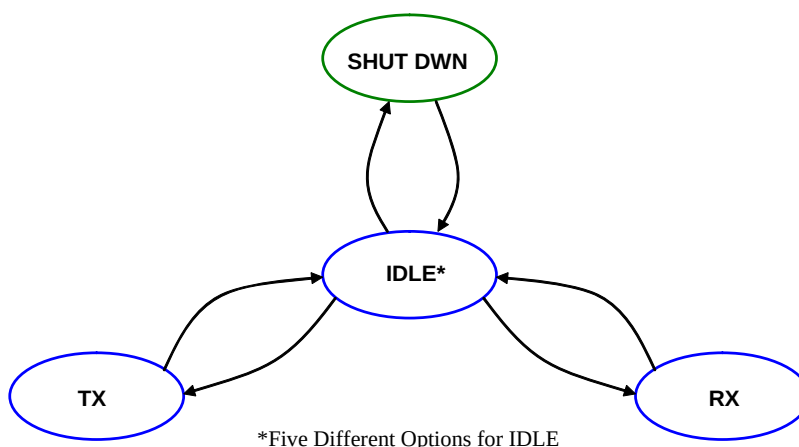


Figure 6. State Machine Diagram

Table 11. Operating Modes

| State/Mode      | xtal | pll | wt | LBDor<br>TS | Response Time to |             | Current in State /Mode<br>[ $\mu$ A] |
|-----------------|------|-----|----|-------------|------------------|-------------|--------------------------------------|
|                 |      |     |    |             | TX               | RX          |                                      |
| Shut Down State | X    | X   | X  | X           | 16.21 ms         | 16.21 ms    | 10 nA                                |
| Idle States:    |      |     |    |             |                  |             |                                      |
| Standby Mode    | 0    | 0   | 0  | 0           | 1.21 ms          | 1.21 ms     | 400 nA                               |
| Sleep Mode      | 0    | 0   | 1  | 0           |                  |             | 800 nA                               |
| Sensor Mode     | 0    | 0   | X  | 1           |                  |             | 1 $\mu$ A                            |
| Ready Mode      | 1    | 0   | X  | X           | 210 $\mu$ s      | 210 $\mu$ s | 600 $\mu$ A                          |
| Tune Mode       | 1    | 1   | X  | X           | 200 $\mu$ s      | 200 $\mu$ s | 9.5 mA                               |
| TX State        | 1    | 1   | X  | X           | NA               | 200 $\mu$ s | 28 mA @ +13 dBm                      |
| RX State        | 1    | 1   | X  | X           | 200 $\mu$ s      | NA          | 18.5 mA                              |

## 3.2.1. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 10 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

## 3.2.2. Idle State

There are five different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 11. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

### 3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption possible with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The standby mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

### 3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.6. Wake-Up Timer" on page 63 for more information on the Wake-Up-Timer. Sleep mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

### 3.2.2.3. SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 and the temperature sensor can be enabled by setting ents = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.4. Temperature Sensor" on page 60 and "8.5. Low Battery Detector" on page 62 for more information on these features. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

### 3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to the TX or RX mode by eliminating the crystal start-up time. Ready mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled. This is done by setting "Register 62h. Crystal Oscillator/Power-on-Reset Control" to a value of 02h. To exit ready mode, bufovr (bit 1) of this register must be set back to 0.

### 3.2.2.5. TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for Frequency Hopping Systems (FHS). Tune mode is entered by setting pllcn = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

### 3.2.3. TX State

The TX state may be entered from any of the IDLE modes when the txon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA to prevent unwanted spectral splatter. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the Main Digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").
5. Wait until PLL settles to required transmit frequency (controlled by timer).
6. Activate Power Amplifier and wait until power ramping is completed (controlled by timer).
7. Transmit Packet.

The first few steps may be eliminated depending on which IDLE mode the chip is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled. If the ambient temperature is constant and the same frequency band is being used these functions may be skipped by setting the appropriate bits in "Register 55h. Calibration Control".

### 3.2.4. RX State

The RX state may be entered from any of the Idle modes when the rxon bit is set to 1 in "Register 07h. Operating Mode and Function Control 1". A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the Main Digital LDO and the Analog LDOs.
2. Start up crystal oscillator and wait until ready (controlled by timer).
3. Enable PLL.
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").
5. Wait until PLL settles to required transmit frequency (controlled by timer).
6. Enable receive circuits: LNA, mixers, and ADC.
7. Calibrate ADC (RC calibration).
8. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

### 3.2.5. Device Status

| Add | R/W | Function/Description | D7     | D6     | D5     | D4      | D3 | D2 | D1     | D0     | POR Def. |
|-----|-----|----------------------|--------|--------|--------|---------|----|----|--------|--------|----------|
| 02  | R   | Device Status        | ffovfl | ffunfl | rxffem | headerr |    |    | cps[1] | cps[0] | —        |

The operational status of the chip can be read from "Register 02h. Device Status".

## 3.3. Interrupts

The Si4431 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has been detected by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h–04h) containing the active Interrupt Status bit; the nIRQ output signal will then be reset until the next change in status is detected. All of the interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h–06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs inside of the chip it will not trigger the nIRQ pin, but the status may still be read correctly at anytime in the Interrupt Status registers.

| Add | R/W | Function/Description | D7      | D6          | D5          | D4          | D3    | D2       | D1        | D0         | POR Def. |
|-----|-----|----------------------|---------|-------------|-------------|-------------|-------|----------|-----------|------------|----------|
| 03  | R   | Interrupt Status 1   | ifferr  | itxffafull  | itxffaem    | irxffafull  | iext  | ipksent  | ipkvalid  | icrcerror  | —        |
| 04  | R   | Interrupt Status 2   | iswdet  | ipreaval    | ipreainval  | irssi       | iwut  | ilbd     | ichiprdy  | ipor       | —        |
| 05  | R/W | Interrupt Enable 1   | enfferr | entxffafull | entxffaem   | enrxffafull | enext | enpksent | enpkvalid | encrcerror | 00h      |
| 06  | R/W | Interrupt Enable 2   | enswdet | enpreaval   | enpreainval | enrssi      | enwut | enlbd    | enchiprdy | enpor      | 01h      |

See “Register 03h. Interrupt/Status 1,” on page 85 and “Register 04h. Interrupt/Status 2,” on page 87 for a complete list of interrupts.

## 3.4. Device Code

The device version code is readable from "Register 01h. Version Code (VC)". This is a read only register.

| Add | R/W | Function/Description | D7 | D6 | D5 | D4    | D3    | D2    | D1    | D0    | POR Def. | Notes |
|-----|-----|----------------------|----|----|----|-------|-------|-------|-------|-------|----------|-------|
| 01  | R   | Device Version       | 0  | 0  | 0  | vc[4] | vc[3] | vc[2] | vc[1] | vc[0] | 00h      | DV    |

### 3.5. System Timing

The system timing for TX and RX modes is shown in Figures 8 and 7. The timing is shown transitioning from STANDBY mode to TX mode and going automatically through the built-in sequencer of required steps. If a small range of frequencies is being used and the temperature range is fairly constant a calibration may only be needed at the initial power up of the device. The relevant system timing registers are shown below.

| Add | R/W | Function/Description | D7         | D6                 | D5              | D4       | D3    | D2            | D1     | D0           | POR Def. |
|-----|-----|----------------------|------------|--------------------|-----------------|----------|-------|---------------|--------|--------------|----------|
| 53  | R/W | PLL Tune Time        | pllts[4:0] |                    |                 |          |       | pllt0[2:0]    |        |              | 45h      |
| 54  | R/W | Reserved 1           | X          | X                  | X               | X        | X     | X             | X      | X            | 00h      |
| 55  | R/W | Calibration Control  |            | xtal-<br>starthalf | adccal-<br>done | enrcfcal | rccal | vco-<br>caldp | vcocal | skip-<br>vco | 04h      |

The VCO will automatically calibrate at every frequency change or power up. The VCO CAL may also be forced by setting the vcocal bit. The 32.768 kHz RC oscillator is also automatically calibrated but the calibration may also be forced. The enrccal will enable the RC Fine Calibration which will occur every 30 seconds. The rccal bit will force a complete calibration of the RC oscillator which will take approximately 2 ms. The PLL T0 time is to allow for bias settling of the VCO, the default for this should be adequate. The PLL TS time is for the settling time of the PLL, which has a default setting of 200  $\mu$ s. This setting should be adequate for most applications but may be reduced if small frequency jumps are used. For more information on the PLL register configuration options, see “Register 53h. PLL Tune Time,” on page 132 and “Register 55h. Calibration Control,” on page 133.

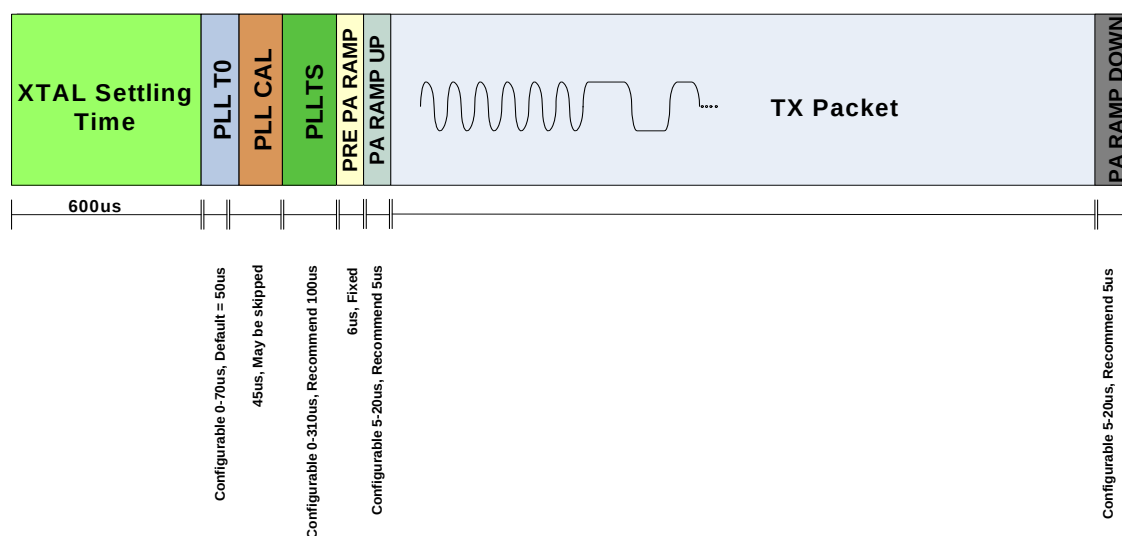


Figure 7. TX Timing

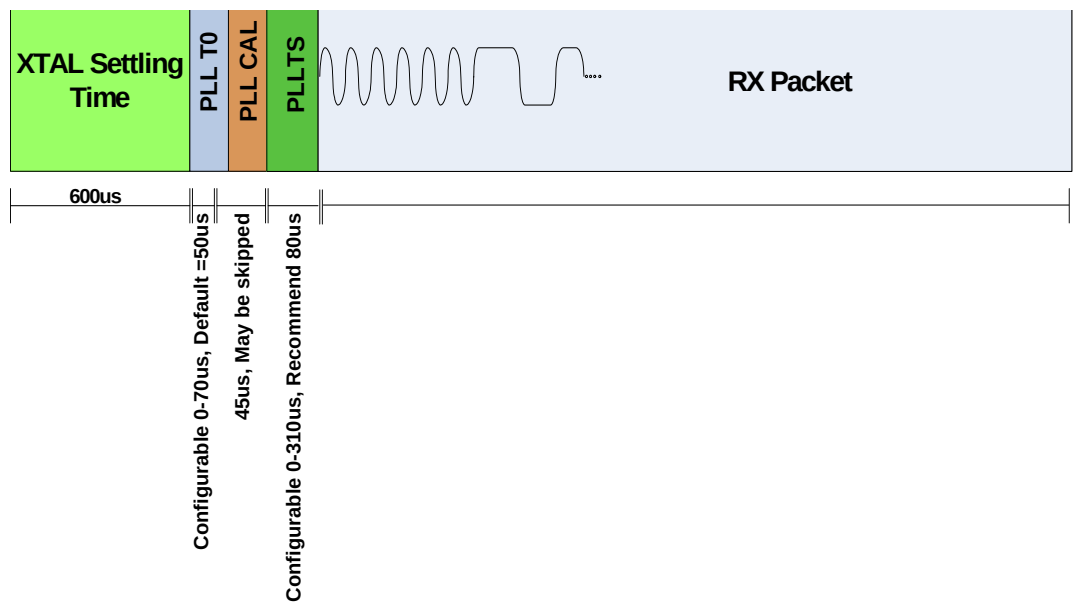


Figure 8. RX Timing

### 3.6. Frequency Control

For calculating the necessary frequency register settings it is recommended to use the easy control window in Silicon Labs' Wireless Design Suite (WDS) or the Excel Calculator available on the product website. These methods offer a simple method to quickly determine the correct settings based on the application requirements. The following information can be used to calculate these values manually.

#### 3.6.1. Frequency Programming

In order to receive or transmit an RF signal, the desired channel frequency,  $f_{\text{carrier}}$ , must be programmed into the Si4431. Note that this frequency is the center frequency of the desired channel and not an LO frequency. The carrier frequency is generated by a Fractional-N Synthesizer, using 10 MHz both as the reference frequency and the clock of the (3<sup>rd</sup> order)  $\Delta\Sigma$  modulator. This modulator uses modulo 64000 accumulators. This design was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consists of an integer part (N) and a fractional part (F). In a generic sense, the output frequency of the synthesizer is:

$$f_{\text{OUT}} = 10\text{MHz} \times (N + F)$$

The fractional part (F) is determined by three different values, Carrier Frequency (fc[15:0]), Frequency Offset (fo[8:0]), and Frequency Modulation (fd[7:0]). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in "3.6.4. Frequency Deviation" on page 29. Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the fc[15:0] register will determine the fractional component. The equation for selection of the carrier frequency is shown below:

$$f_{\text{carrier}} = 10\text{MHz} \times (\text{hbsel} + 1) \times (N + F)$$

$$f_{\text{TX}} = 10\text{MHz} * (\text{hbsel} + 1) * (\text{fb}[4:0] + 24 + \frac{\text{fc}[15:0]}{64000})$$

| Add | R/W | Function/Description        | D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    | POR Def. |
|-----|-----|-----------------------------|--------|--------|--------|--------|--------|--------|-------|-------|----------|
| 73  | R/W | Frequency Offset 1          | fo[7]  | fo[6]  | fo[5]  | fo[4]  | fo[3]  | fo[2]  | fo[1] | fo[0] | 00h      |
| 74  | R/W | Frequency Offset 2          |        |        |        |        |        |        | fo[9] | fo[8] | 00h      |
| 75  | R/W | Frequency Band Select       |        | sbsel  | hbsel  | fb[4]  | fb[3]  | fb[2]  | fb[1] | fb[0] | 35h      |
| 76  | R/W | Nominal Carrier Frequency 1 | fc[15] | fc[14] | fc[13] | fc[12] | fc[11] | fc[10] | fc[9] | fc[8] | BBh      |
| 77  | R/W | Nominal Carrier Frequency 0 | fc[7]  | fc[6]  | fc[5]  | fc[4]  | fc[3]  | fc[2]  | fc[1] | fc[0] | 80h      |

The integer part (N) is determined by fb[4:0]. Additionally, the output frequency can be halved by connecting a ÷2 divider to the output. This divider is not inside the loop and is controlled by the hbsel bit in "Register 75h. Frequency Band Select". This effectively partitions the entire 240–930 MHz frequency range into two separate bands: High Band (HB) for hbsel = 1, and Low Band (LB) for hbsel = 0. The valid range of fb[4:0] is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. Table 12 demonstrates the selection of fb[4:0] for the corresponding frequency band.

After selection of the fb (N) the fractional component may be solved with the following equation:

$$\text{fc}[15:0] = \left( \frac{f_{\text{TX}}}{10\text{MHz} * (\text{hbsel} + 1)} - \text{fb}[4:0] - 24 \right) * 64000$$

fb and fc are the actual numbers stored in the corresponding registers.

Table 12. Frequency Band Selection

| fb[4:0] Value | N  | Frequency Band |               |
|---------------|----|----------------|---------------|
|               |    | hbsel=0        | hbsel=1       |
| 0             | 24 | 240–249.9 MHz  | 480–499.9 MHz |
| 1             | 25 | 250–259.9 MHz  | 500–519.9 MHz |
| 2             | 26 | 260–269.9 MHz  | 520–539.9 MHz |
| 3             | 27 | 270–279.9 MHz  | 540–559.9 MHz |
| 4             | 28 | 280–289.9 MHz  | 560–579.9 MHz |
| 5             | 29 | 290–299.9 MHz  | 580–599.9 MHz |
| 6             | 30 | 300–309.9 MHz  | 600–619.9 MHz |
| 7             | 31 | 310–319.9 MHz  | 620–639.9 MHz |
| 8             | 32 | 320–329.9 MHz  | 640–659.9 MHz |
| 9             | 33 | 330–339.9 MHz  | 660–679.9 MHz |
| 10            | 34 | 340–349.9 MHz  | 680–699.9 MHz |
| 11            | 35 | 350–359.9 MHz  | 700–719.9 MHz |
| 12            | 36 | 360–369.9 MHz  | 720–739.9 MHz |
| 13            | 37 | 370–379.9 MHz  | 740–759.9 MHz |
| 14            | 38 | 380–389.9 MHz  | 760–779.9 MHz |
| 15            | 39 | 390–399.9 MHz  | 780–799.9 MHz |
| 16            | 40 | 400–409.9 MHz  | 800–819.9 MHz |
| 17            | 41 | 410–419.9 MHz  | 820–839.9 MHz |
| 18            | 42 | 420–429.9 MHz  | 840–859.9 MHz |
| 19            | 43 | 430–439.9 MHz  | 860–879.9 MHz |
| 20            | 44 | 440–449.9 MHz  | 880–899.9 MHz |
| 21            | 45 | 450–459.9 MHz  | 900–919.9 MHz |
| 22            | 46 | 460–469.9 MHz  | 920–930.0 MHz |
| 23            | 47 | 470–479.9 MHz  | —             |

The chip will automatically shift the frequency of the Synthesizer down by 937.5 kHz ( $30 \text{ MHz} \div 32$ ) to achieve the correct Intermediate Frequency (IF) when RX mode is entered. Low-side injection is used in the RX Mixing architecture; therefore, no frequency reprogramming is required when using the same TX frequency and switching between RX/TX modes.

### 3.6.2. Easy Frequency Programming for FHSS

While Registers 73h–77h may be used to program the carrier frequency of the Si4431, it is often easier to think in terms of “channels” or “channel numbers” rather than an absolute frequency value in Hz. Also, there may be some timing-critical applications (such as for Frequency Hopping Systems) in which it is desirable to change frequency by programming a single register. Once the channel step size is set, the frequency may be changed by a single register corresponding to the channel number. A nominal frequency is first set using Registers 73h–77h, as described above. Registers 79h and 7Ah are then used to set a channel step size and channel number, relative to the nominal setting. The Frequency Hopping Step Size (fhs[7:0]) is set in increments of 10 kHz with a maximum channel step size of 2.56 MHz. The Frequency Hopping Channel Select Register then selects channels based on multiples of the step size.

$$F_{\text{carrier}} = F_{\text{nom}} + fhs[7:0] \times (fhch[7:0] \times 10\text{kHz})$$

For example: if the nominal frequency is set to 900 MHz using Registers 73h–77h and the channel step size is set to 1 MHz using "Register 7Ah. Frequency Hopping Step Size". For example, if the "Register 79h. Frequency Hopping Channel Select" is set to 5d, the resulting carrier frequency would be 905 MHz. Once the nominal frequency and channel step size are programmed in the registers, it is only necessary to program the fhch[7:0] register in order to change the frequency.

| Add | R/W | Function/Description             | D7      | D6      | D5      | D4      | D3      | D2      | D1      | D0      | POR Def. |
|-----|-----|----------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|----------|
| 79  | R/W | Frequency Hopping Channel Select | fhch[7] | fhch[6] | fhch[5] | fhch[4] | fhch[3] | fhch[2] | fhch[1] | fhch[0] | 00h      |
| 7A  | R/W | Frequency Hopping Step Size      | fhs[7]  | fhs[6]  | fhs[5]  | fhs[4]  | fhs[3]  | fhs[2]  | fhs[1]  | fhs[0]  | 00h      |

### 3.6.3. Automatic Frequency Change

If registers 79h or 7Ah are changed in either TX or mode, the state machine will automatically transition the chip back to tune, change the frequency, and automatically go back to either TX or RX. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. This in turn reduces microcontroller activity, reducing current consumption.

### 3.6.4. Frequency Deviation

The peak frequency deviation is configurable from  $\pm 1$  to  $\pm 320$  kHz. The Frequency Deviation ( $\Delta f$ ) is controlled by the Frequency Deviation Register (fd), address 71 and 72h, and is independent of the carrier frequency setting. When enabled, regardless of the setting of the hbsel bit (high band or low band), the resolution of the frequency deviation will remain in increments of 625 Hz. When using frequency modulation the carrier frequency will deviate from the nominal center channel carrier frequency by  $\pm \Delta f$ :

$$\Delta f = fd[8:0] \times 625\text{Hz}$$

$$fd[8:0] = \frac{\Delta f}{625\text{Hz}} \quad \Delta f = \text{peak deviation}$$

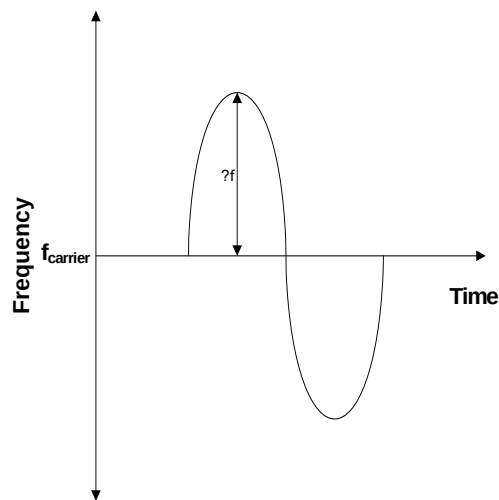


Figure 9. Frequency Deviation

The previous equation should be used to calculate the desired frequency deviation. If desired, frequency modulation may also be disabled in order to obtain an unmodulated carrier signal at the channel center frequency; see "4.1. Modulation Type" on page 34 for further details.

| Add | R/W | Function/Description      | D7       | D6       | D5       | D4       | D3    | D2    | D1        | D0        | POR Def. |
|-----|-----|---------------------------|----------|----------|----------|----------|-------|-------|-----------|-----------|----------|
| 71  | R/W | Modulation Mode Control 2 | trclk[1] | trclk[0] | dtmod[1] | dtmod[0] | eninv | fd[8] | modtyp[1] | modtyp[0] | 00h      |
| 72  | R/W | Frequency Deviation       | fd[7]    | fd[6]    | fd[5]    | fd[4]    | fd[3] | fd[2] | fd[1]     | fd[0]     | 43h      |

### 3.6.5. Frequency Offset Adjustment

When the AFC is disabled the frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The frequency offset adjustment and the AFC both are implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register so in order to get a negative offset you will need to take the two's complement of the positive offset number. The offset can be calculated by the following:

$$\text{DesiredOffset} = 156.25\text{Hz} \times (\text{hbsel} + 1) \times \text{fo}[9:0]$$

$$\text{fo}[9:0] = \frac{\text{DesiredOffset}}{156.25\text{Hz} \times (\text{hbsel} + 1)}$$

The adjustment range in high band is:  $\pm 160$  kHz, and adjustment range in low band is:  $\pm 80$  kHz. For example to compute an offset of +50 kHz in high band mode fo[9:0] should be set to 0A0h. For an offset of -50 kHz in high band mode the fo[9:0] register should be set to 360h.

When AFC is enabled the same registers can be used to read the offset value as automatically obtained by the AFC. A stable offset value can read after preamble detection using the preamble detection or sync word detection interrupt.

| Add | R/W | Function/Description | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    | POR Def. | Notes |
|-----|-----|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------|-------|
| 73  | R/W | Frequency Offset     | fo[7] | fo[6] | fo[5] | fo[4] | fo[3] | fo[2] | fo[1] | fo[0] | 00h      | 73    |
| 74  | R/W | Frequency Offset     |       |       |       |       |       |       | fo[9] | fo[8] | 00h      |       |

### 3.6.6. Auto Frequency Control (AFC)

The receiver supports automatic frequency control (AFC) to compensate for frequency differences between the transmitter and receiver reference frequencies. These differences can be caused by the absolute accuracy and temperature dependencies of the reference crystals. Due to frequency offset compensation in the modem, the receiver is tolerant to frequency offsets up to 0.25 times the IF bandwidth when the AFC is disabled. When the AFC is enabled, the received signal will be centered in the pass-band of the IF filter, providing optimal sensitivity and selectivity over a wider range of frequency offsets up to 0.35 times the IF bandwidth. The trade-off of receiver sensitivity (at 1% PER) versus carrier offset and the impact of AFC are illustrated in Figure 10.

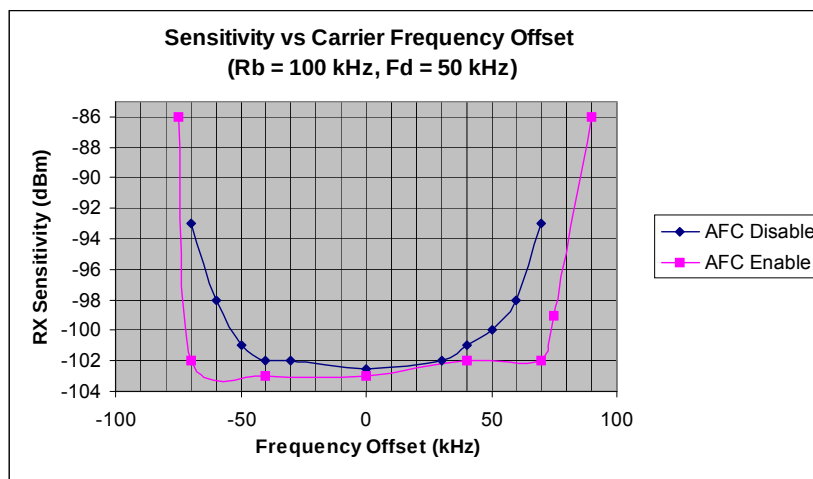


Figure 10. Sensitivity at 1% PER vs. Carrier Frequency Offset

The AFC function shares registers 73h and 74h with the Frequency Offset setting. If AFC is enabled (D6 in "Register 1Dh. AFC Loop Gearshift Override," on page 105), the Frequency Offset shows the results of the AFC algorithm for the current receive slot. When selecting the preamble length, the length needs to be long enough to settle the AFC. In general two bytes of preamble is sufficient to settle the AFC. Disabling the AFC allows the preamble to be shortened by about 8 bits. Note that with the AFC disabled, the preamble length must still be long enough to settle the receiver and to detect the preamble (see "6.7. Preamble Length" on page 47). The AFC corrects the detected frequency offset by changing the frequency of the Fractional-N PLL. When the preamble is detected, the AFC will freeze. In multi-packet mode the AFC is reset at the end of every packet and will re-acquire the frequency offset for the next packet. An automatic reset circuit prevents excessive drift by resetting the AFC loop when the tuning exceeds 2 times the frequency deviation (as set by fd[8:0] in register 71h and 72h) in high band or 1 times the frequency deviation in low band. This range can be halved by the "afcbd" bit in register 1Dh. If needed, fd[8:0] can have a different value in RX mode compared to TX mode.

In TX mode, the "Register 73h. Frequency Offset 1" is used to provide an offset to the programmed transmit frequency. This offset allows fine tuning of the transmit frequency to account for the variability of the TX reference frequency. Note that reading this register shows the frequency offset calculated from the last AFC action, not what was previously written to the Frequency Offset register.

The amount of feedback to the Fractional-N PLL before the preamble is detected is controlled from afcgearh[2:0]. The default value 000 relates to a feedback of 100% from the measured frequency error and is advised for most applications. Every bit added will half the feedback but will require a longer preamble to settle. The amount of feedback after the preamble is detected is controlled from afcgearl[2:0].

The AFC operates as follows. The frequency error of the incoming signal is measured over a period of two bit times, after which it corrects the local oscillator via the Fractional-N PLL. After this correction, some time is allowed to settle the Fractional-N PLL to the new frequency before the next frequency error is measured. The duration of the AFC cycle before the preamble is detected can be programmed with shwait[2:0] ("Register 1Eh. AFC Timing Control," on page 106). It is advised to use the default value 001, which sets the AFC cycle to 4 bit times (2 for measurement and 2 for settling). The duration of the AFC cycle after the preamble detection and before the end of the preamble can be programmed with lgwait[2:0]. It is advised to use the default value 000 such that the AFC is disabled after the preamble is detected.

|              | Frequency Correction |                      |
|--------------|----------------------|----------------------|
|              | RX                   | TX                   |
| AFC disabled | Freq Offset Register | Freq Offset Register |
| AFC enabled  | AFC                  | Freq Offset Register |

| Add | R/W | Function/Description        | D7    | D6     | D5          | D4          | D3          | D2          | D1          | D0          | POR Def. |
|-----|-----|-----------------------------|-------|--------|-------------|-------------|-------------|-------------|-------------|-------------|----------|
| 1D  | R/W | AFC Loop Gearshift Override | afcbd | enaafc | afcgearh[2] | afcgearh[1] | afcgearh[0] | afcgearl[2] | afcgearl[1] | afcgearl[0] | 40h      |

### 3.6.7. TX Data Rate Generator

The data rate is configurable between 1–128 kbps. For data rates below 30 kbps the "txdtrtscale" bit in register 70h should be set to 1. When higher data rates are used this bit should be set to 0.

The TX data rate is determined by the following formula:

$$DR\_TX = \frac{txdr[15:0] \times 1MHz}{2^{16+5 \cdot txdtrtscale}}$$

$$txdr[15:0] = \frac{DR\_TX \times 2^{16+5 \cdot txdtrtscale}}{1MHz}$$

The txdr register may be found in the following registers.

| Add | R/W | Function/Description | D7       | D6       | D5       | D4       | D3       | D2       | D1      | D0      | POR Def. |
|-----|-----|----------------------|----------|----------|----------|----------|----------|----------|---------|---------|----------|
| 6E  | R/W | TX Data Rate 1       | txdr[15] | txdr[14] | txdr[13] | txdr[12] | txdr[11] | txdr[10] | txdr[9] | txdr[8] | 0Ah      |
| 6F  | R/W | TX Data Rate 0       | txdr[7]  | txdr[6]  | txdr[5]  | txdr[4]  | txdr[3]  | txdr[2]  | txdr[1] | txdr[0] | AAh      |

4. Modulation Options

4.1. Modulation Type

The Si4431 supports three different modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), and On-Off Keying (OOK). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. Figure 11 demonstrates the difference between FSK and GFSK for a Data Rate of 64 kbps. The time domain plots demonstrate the effects of the Gaussian filtering. The frequency domain plots demonstrate the spectral benefit of GFSK over FSK. The type of modulation is selected with the modtyp[1:0] bits in "Register 71h. Modulation Mode Control 2". Note that it is also possible to obtain an unmodulated carrier signal by setting modtyp[1:0] = 00.

| modtyp[1:0] | Modulation Source                                  |
|-------------|----------------------------------------------------|
| 00          | Unmodulated Carrier                                |
| 01          | OOK                                                |
| 10          | FSK                                                |
| 11          | GFSK (enable TX Data CLK when direct mode is used) |

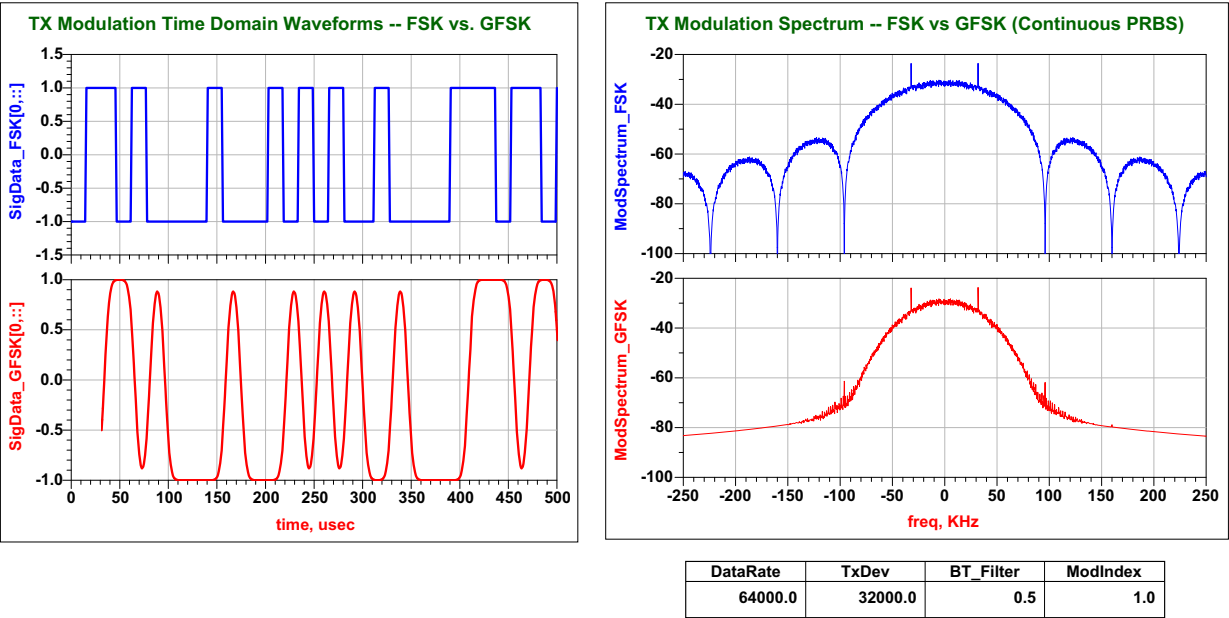


Figure 11. FSK vs GFSK Spectrums

## 4.2. Modulation Data Source

The Si4431 may be configured to obtain its modulation data from one of three different sources: FIFO mode, Direct Mode, and from a PN9 mode. Furthermore, in Direct Mode, the TX modulation data may be obtained from several different input pins. These options are set through the dtmod[1:0] field in "Register 71h. Modulation Mode Control 2".

| Add | R/W | Function/Description      | D7       | D6       | D5       | D4       | D3    | D2    | D1        | D0        | POR Def. |
|-----|-----|---------------------------|----------|----------|----------|----------|-------|-------|-----------|-----------|----------|
| 71  | R/W | Modulation Mode Control 2 | trclk[1] | trclk[0] | dtmod[1] | dtmod[0] | eninv | fd[8] | modtyp[1] | modtyp[0] | 23h      |

| dtmod[1:0] | Modulation Source                                                                |
|------------|----------------------------------------------------------------------------------|
| 00         | Direct Mode using TX_Data via GPIO pin (GPIO needs programming accordingly also) |
| 01         | Direct Mode using TX_Data via SDI pin (only when nSEL is high)                   |
| 10         | FIFO Mode                                                                        |
| 11         | PN9 (internally generated)                                                       |

## 4.3. FIFO Mode

In FIFO mode, the integrated FIFOs are used to transmit and receive the data. The FIFOs are accessed via "Register 7Fh. FIFO Access" with burst read/write capability. The FIFOs may be configured specific to the application packet size, etc. (see "6. Data Handling and Packet Handler" on page 42 for further information).

When in FIFO mode the chip will automatically exit the TX or RX State when either the *ipksent* or *ipkvalid* interrupt occurs. The chip will return to any of the other states based on the settings in "Register 07h. Operating Mode and Function Control 1". For instance, if the chip is put into TX mode and both the txon and pll on bits are set, the chip will transmit all of the contents of the FIFO and the ipksent interrupt will occur. When this event occurs the chip will clear the txon bit and return to pll on or Tune Mode. If no other bits are set in register 07h besides txon initially then the chip will return to the Idle state.

In RX mode the rxon bit will only be cleared if ipkvalid occurs. A CRC, Header, or Sync error will generate an interrupt and the microcontroller will need to decide on the next action.

## 4.4. Direct Mode

For legacy systems that have packet handling within an MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct Mode is provided which bypasses the FIFOs entirely. In Direct Mode, the TX modulation data is applied to an input pin of the chip and processed in "real time" (i.e., not stored in a register for transmission at a later time). There are various configurations for choosing which pin is used for the TX Data. Furthermore, an additional input pin is required for the TX Data Clock if GFSK modulation is desired (only the TX Data input pin is required for FSK). Two options for the source of the TX Data are available in the dtmod[1:0] field, and various configurations for the source of the TX Data Clock may be selected through the trclk[1:0] field.

| trclk[1:0] | TX Data Clock Configuration                                                      |
|------------|----------------------------------------------------------------------------------|
| 00         | No TX Clock (only for FSK)                                                       |
| 01         | TX Data Clock is available via GPIO (GPIO needs programming accordingly as well) |
| 10         | TX Data Clock is available via SDO pin (only when nSEL is high)                  |
| 11         | TX Data Clock is available via the nIRQ pin                                      |

The eninv bit in Address 71h will invert the TX Data for testing purposes.

## 4.5. PN9 Mode

In this mode the TX Data is generated internally using a pseudorandom (PN9 sequence) bit generator. The primary purpose of this mode is for use as a test mode to observe the modulated spectrum without having to load/provide data.

## 4.6. Synchronous vs. Asynchronous

In Asynchronous mode no clock is used to synchronize the data to the internal modulator. This mode can only be used with FSK. The advantage of this mode is that it saves a microcontroller pin because no data clock is required. The disadvantage is that you don't get the clean spectrum and limited BW of GFSK. If Asynchronous FSK is used the TX\_DR register should be set to its maximum value.

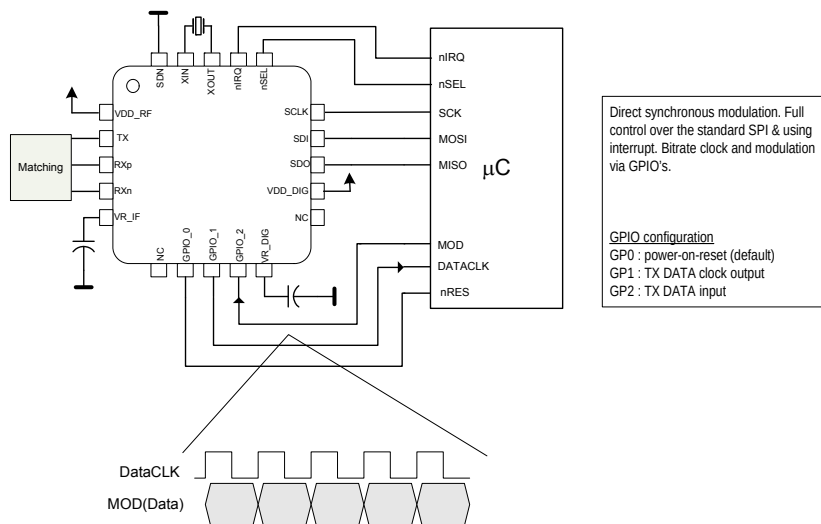


**Figure 12. Direct Synchronous Mode Example**

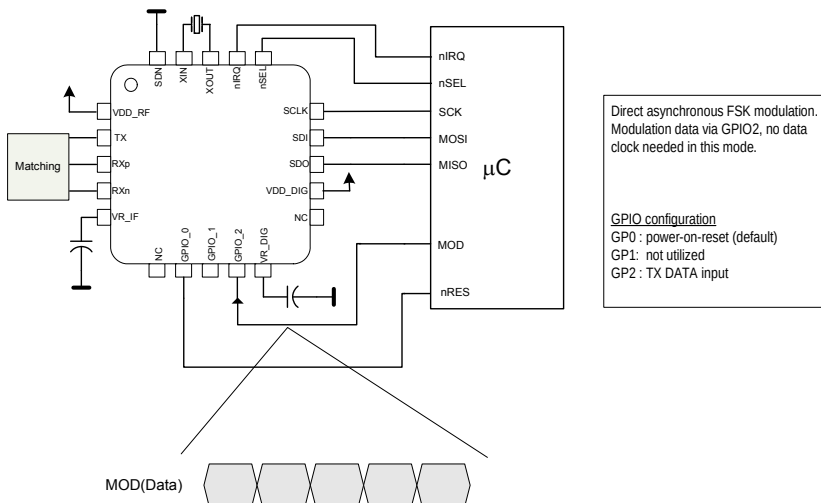
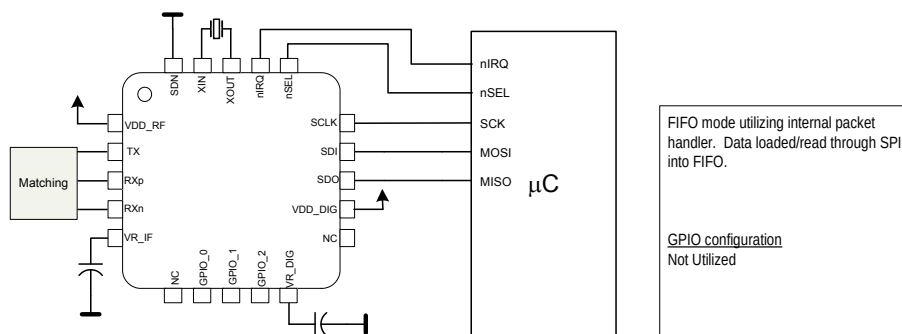


**Figure 13. Direct Asynchronous Mode Example**

**Figure 14. FIFO Mode Example**

## 5. Internal Functional Blocks

This section provides an overview some of the key blocks of the internal radio architecture.

### 5.1. RX LNA

The input frequency range for the LNA is 240–930 MHz. The LNA provides gain with a noise figure low enough to suppress the noise of the following stages. The LNA has one step of gain control which is controlled by the analog gain control (AGC) algorithm. The AGC algorithm adjusts the gain of the LNA and PGA so the receiver can handle signal levels from sensitivity to +5 dBm with optimal performance.

### 5.2. RX I-Q Mixer

The output of the LNA is fed internally to the input of the receive mixer. The receive mixer is implemented as an I-Q mixer that provides both I and Q channel outputs to the programmable gain amplifier. The mixer consists of two double-balanced mixers whose RF inputs are driven in parallel, local oscillator (LO) inputs are driven in quadrature, and separate I and Q Intermediate Frequency (IF) outputs drive the programmable gain amplifier. The receive LO signal is supplied by an integrated VCO and PLL synthesizer operating between 240–930 MHz. The necessary quadrature LO signals are derived from the divider at the VCO output.

### 5.3. Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) provides the necessary gain to boost the signal level into the Dynamic Range of the ADC. The PGA must also have enough gain switching to allow for large input signals to ensure a linear RSSI range up to –20 dBm. The PGA is designed to have steps of 3 dB which are controlled by the AGC algorithm in the digital modem.

### 5.4. ADC

The amplified I&Q IF signals are digitized using an Analog-to-Digital Converter (ADC), which allows for low current consumption and high dynamic range. The bandpass response of the ADC provides exceptional rejection of out of band blockers.

### 5.5. Digital Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain, resulting in reduced area while increasing flexibility. The digital modem performs the following functions:

- Channel Selection Filter
- TX Modulation
- RX Demodulation
- AGC
- Preamble Detector
- Invalid Preamble Detector
- Radio Signal Strength Indicator (RSSI)
- Automatic Frequency Compensation (AFC)
- Packet Handling including EZMac™ features
- Cyclic Redundancy Check (CRC)

The digital Channel Filter and Demodulator are optimized for ultra low power consumption and are highly configurable. Supported modulation types are GFSK, FSK, and OOK. The Channel Filter can be configured to support a large choice of bandwidths ranging from 620 kHz down to 2.6 kHz. A large variety of data rates are supported ranging from 1 up to 128 kbps. The AGC algorithm is implemented digitally using an advanced control loop optimized for fast response time.

The configurable Preamble Detector is used to improve the reliability of the Sync-word detection. The Sync-word detector is only enabled when a valid preamble is detected, significantly reducing the probability of false Sync-word detection.

The Invalid Preamble Detector issues an interrupt when no valid preamble signal is found. After the receiver is enabled, the Invalid Preamble Detector output is ignored for 16 Tb (Where Tb is the time of a bit duration) to allow the receiver to settle. The Invalid Preamble Detect interrupt can be used to save power and speed-up search in receive mode. It is advised to mask the invalid preamble interrupt when Antenna Diversity is enabled.

The Received Signal Strength Indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI is 0.5 dB. This high resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), carrier sense (CS), and listen before talk (LBT) functionality.

Frequency mistuning caused by crystal inaccuracies can be compensated by enabling the digital Automatic Frequency Control (AFC) in receive mode.

A comprehensive programmable Packet Handler including key features of Silicon Labs' EZMac™ is integrated to create a variety of communication topologies ranging from peer-to-peer networks to mesh networks. The extensive programmability of the packet header allows for advanced packet filtering which in turn enables a mix of broadcast, group, and point-to-point communication.

A wireless communication channel can be corrupted by noise and interference, and it is therefore important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the tail of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The Packet Handler and CRC are extremely valuable features which can significantly reduce the load on the system microcontroller allowing for a simpler and cheaper microcontroller.

The digital modem includes the TX Modulator which converts the TX Data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK, considerably reducing the energy in the adjacent channels. The bandwidth-time product (BT) is 0.5 for all programmed data rates.

## 5.6. Synthesizer

An integrated Sigma Delta ( $\Sigma\Delta$ ) Fractional-N PLL synthesizer capable of operating from 240–930 MHz is provided on-chip. Using a  $\Sigma\Delta$  synthesizer has many advantages; it provides large amounts of flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider which results in very precise accuracy and control over the transmit deviation.

The PLL and  $\Delta\text{-}\Sigma$  modulator scheme is designed to support any desired frequency and channel spacing in the range from 240–930 MHz with a frequency resolution of 156.25 Hz (Low band) or 312.5 Hz (High band). The transmit data rate can be programmed between 1–128 kbps, and the frequency deviation can be programmed between  $\pm 1\text{--}160$  kHz. These parameters may be adjusted via registers as shown in "3.6. Frequency Control" on page 27.

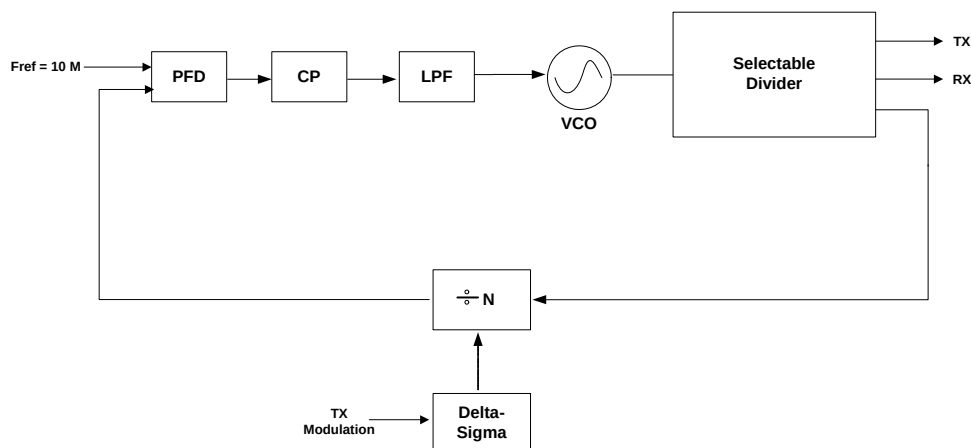


Figure 15. PLL Synthesizer Block Diagram

The reference frequency to the PLL is 10 MHz. The PLL utilizes a differential L-C VCO, with integrated on-chip spiral inductors. The output of the VCO is followed by a configurable divider which will divide down the signal to the desired output frequency band. The modulus of this divider stage is controlled dynamically by the output from the  $\Delta$ - $\Sigma$  modulator. The tuning resolution of the  $\Delta$ - $\Sigma$  modulator is determined largely by the over-sampling rate and the number of bits carried internally. The tuning resolution is sufficient to tune to the commanded frequency with a maximum accuracy of 312.5 Hz anywhere in the range between 240–930 MHz.

## 5.6.1. VCO

The output of the VCO is automatically divided down to the correct output frequency depending on the hbsel and fb[4:0] fields in "Register 75h. Frequency Band Select". A 2X VCO is utilized to help avoid problems due to frequency pulling, especially when turning on the integrated Power Amplifier. In receive mode, the LO frequency is automatically shifted downwards (without reprogramming) by the IF frequency of 937.5 kHz, allowing transmit and receive operation on the same frequency. The VCO integrates the resonator inductor, tuning varactor, so no external VCO components are required.

The VCO uses capacitance bank to cover the wide frequency range specified. The capacitance bank will automatically be calibrated every time the synthesizer is enabled. In certain fast hopping applications this might not be desirable so the VCO calibration may be skipped by setting the appropriate register.

## 5.7. Power Amplifier

The Si4431 contains an internal integrated power amplifier (PA) capable of transmitting at output levels between –8 to +13 dBm. The output power is programmable in 3 dB steps through the txpow[2:0] field in "Register 6Dh. TX Power".

The PA design is single-ended and is implemented as a two stage class CE amplifier with efficiency in the range of 45–50% while transmitting at maximum power. The efficiency drops to approximately 20% when operating at the lowest power steps. Due to the high efficiency a simple filter is required on the board to filter the harmonics. The PA output is ramped up and down to prevent unwanted spectral splatter.

### 5.7.1. Output Power Selection

The output power is configurable in 3 dB steps from –8 to +13 dBm with the txpow[2:0] field in "Register 6Dh. TX Power". The PA output is ramped up and down to prevent unwanted spectral splatter.

Extra output power can allow use of a cheaper smaller antenna, greatly reducing the overall BOM cost. The higher power setting of the chip achieves maximum possible range, but of course comes at the cost of higher TX current consumption. However, depending on the duty cycle of the system, the effect on battery life may be insignificant. Contact Silicon Labs Support for help in evaluating this tradeoff.

| Add | R/W | Function/Description | D7 | D6 | D5 | D4 | D3 | D2       | D1       | D0       | POR Def. |
|-----|-----|----------------------|----|----|----|----|----|----------|----------|----------|----------|
| 6D  | R/W | TX Power             |    |    |    |    |    | txpow[2] | txpow[1] | txpow[0] | 07h      |

| txpow[2:0] | Output Power |
|------------|--------------|
| 000        | –8 dBm       |
| 001        | –5 dBm       |
| 010        | –2 dBm       |
| 011        | +1 dBm       |
| 100        | +4 dBm       |
| 101        | +7 dBm       |
| 110        | +10 dBm      |
| 111        | +13 dBm      |

## 5.8. Crystal Oscillator

The Si4431 includes an integrated 30 MHz crystal oscillator with a fast start-up time of less than 600  $\mu$ s when a suitable parallel resonant crystal is used. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the 30 MHz crystal blank.

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the xlc[6:0] field of "Register 09h. 30 MHz Crystal Oscillator Load Capacitance". The total internal capacitance is 12.5 pF and is adjustable in approximately 127 steps (97fF/step). The xtalshift bit is a course shift in frequency but is not binary with xlc[6:0].

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to slightly adjust the frequency of the crystal oscillator. This latter function can be used to compensate for crystal production tolerances. Utilizing the on-chip temperature sensor and suitable control software even the temperature dependency of the crystal can be canceled.

The crystal load capacitance is programmed using register 09h. The typical value of the total on-chip (internal) capacitance C<sub>int</sub> can be calculated as follows:

$$C_{int} = 1.8 \text{ pF} + 0.085 \text{ pF} \times \text{xlc}[6:0] + 3.7 \text{ pF} \times \text{xtalshift}$$

Note that the course shift bit xtalshift is not binary with xlc[6:0]. The total load capacitance C<sub>load</sub> seen by the crystal can be calculated by adding the sum of all external parasitic PCB capacitances C<sub>ext</sub> to C<sub>int</sub>. If the maximum value of C<sub>int</sub> (16.3 pF) is not sufficient, an external capacitor can be added for exact tuning. See more on this, calculating C<sub>ext</sub> and crystal selection guidelines in "11. Application Notes" on page 78.

If AFC is disabled then the synthesizer frequency may be further adjusted by programming the Frequency Offset field fo[9:0] in "Register 73h. Frequency Offset 1" and "Register 74h. Frequency Offset 2", as discussed in "3.6. Frequency Control" on page 27.

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through one of the GPIO pins for use as the System Clock. In this fashion, only one crystal oscillator is required for the entire system and the BOM cost is reduced. The available clock frequencies (i.e., internal division ratios) and the GPIO configuration are discussed further in "8.2. Microcontroller Clock" on page 56.

The Si4431 may also be driven with an external 30 MHz clock signal through the XIN pin.

| Add | R/W | Function/Description                | D7        | D6     | D5     | D4     | D3     | D2     | D1     | D0     | POR Def. |
|-----|-----|-------------------------------------|-----------|--------|--------|--------|--------|--------|--------|--------|----------|
| 09  | R/W | Crystal Oscillator Load Capacitance | xtalshift | xlc[6] | xlc[5] | xlc[4] | xlc[3] | xlc[2] | xlc[1] | xlc[0] | 40h      |

## 5.9. Regulators

There are a total of six regulators integrated onto the Si4431. With the exception of the IF and Digital all regulators are designed to operate with only internal decoupling. The IF and Digital regulators both require an external 1  $\mu$ F decoupling capacitor. All of the regulators are designed to operate with an input supply voltage from +1.8 to +3.6 V, and produce a nominal regulated output voltage of +1.7 V  $\pm$ 5%. The internal circuitry nominally operates from this regulated +1.7 V supply. The output stage of the of PA is not connected internally to a regulator and is connected directly to the battery voltage.

A supply voltage should only be connected to the VDD pins. No voltage should be forced on the IF or DIG regulator outputs.

## 6. Data Handling and Packet Handler

### 6.1. RX and TX FIFOs

Two 64 byte FIFOs are integrated into the chip, one for RX and one for TX, as shown in Figure 16. "Register 7Fh. FIFO Access" is used to access both FIFOs. A burst write, as described in "3.1. Serial Peripheral Interface (SPI)" on page 19, to address 7Fh will write data to the TX FIFO. A burst read from address 7Fh will read data from the RX FIFO.

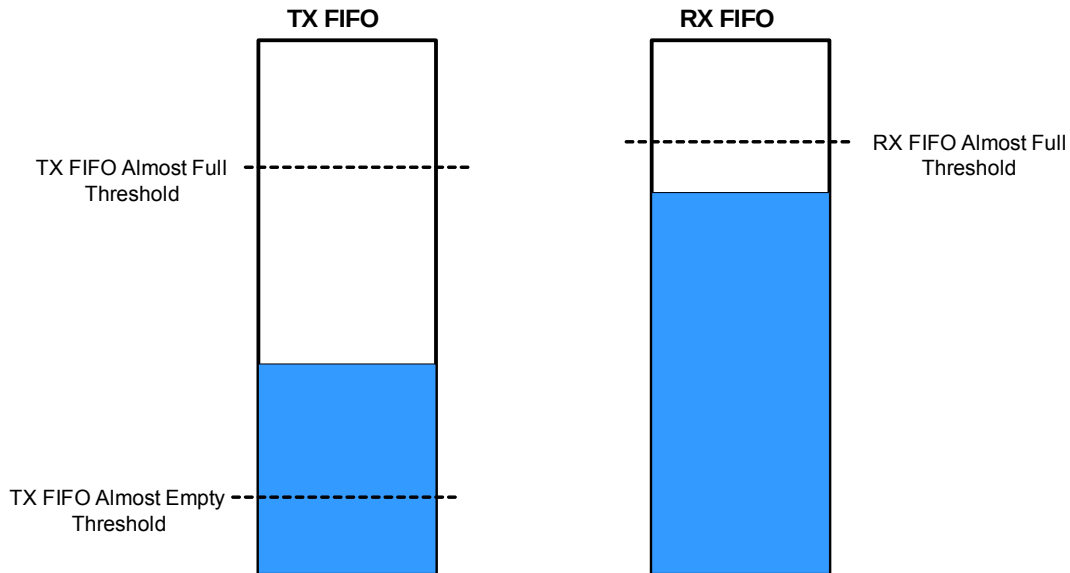


**Figure 16. FIFO Thresholds**

The TX FIFO has two programmable thresholds. An interrupt event occurs when the data in the TX FIFO reaches these thresholds. The first threshold is the FIFO Almost Full threshold, `txafthr[5:0]`. The value in this register corresponds to the desired threshold value in number of bytes. When the data being filled into the TX FIFO reaches this threshold limit, an interrupt to the microcontroller is generated so the chip can enter TX mode to transmit the contents of the TX FIFO. The second threshold for TX is the FIFO Almost Empty Threshold, `txaethr[5:0]`. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold an interrupt will be generated. The microcontroller will need to switch out of TX mode or fill more data into the TX FIFO. The Transceiver may be configured so that when the TX FIFO is empty the chip will automatically move to the Ready state. In this mode the TX FIFO Almost Empty Threshold may not be useful. This functionality is set by the `ffidle` bit in "Register 08h. Operating Mode and Function Control 2," on page 92.

| Add | R/W | Function/Description           | D7        | D6        | D5         | D4         | D3         | D2         | D1         | D0         | POR Def. |
|-----|-----|--------------------------------|-----------|-----------|------------|------------|------------|------------|------------|------------|----------|
| 08  | R/W | Operating & Function Control 2 | antdiv[2] | antdiv[1] | antdiv[0]  | rxmpk      | autotx     | enldm      | ffclrx     | ffclrtx    | 00h      |
| 7C  | R/W | TX FIFO Control 1              |           |           | txafthr[5] | txafthr[4] | txafthr[3] | txafthr[2] | txafthr[1] | txafthr[0] | 37h      |
| 7D  | R/W | TX FIFO Control 2              |           |           | txaethr[5] | txaethr[4] | txaethr[3] | txaethr[2] | txaethr[1] | txaethr[0] | 04h      |

The RX FIFO has one programmable threshold called the FIFO Almost Full Threshold, rxafthr[5:0]. When the incoming RX data reaches the Almost Full Threshold an interrupt will be generated to the microcontroller via the nIRQ pin. The microcontroller will then need to read the data from the RX FIFO.

| Add | R/W | Function/Description | D7       | D6       | D5         | D4         | D3         | D2         | D1         | D0         | POR Def. |
|-----|-----|----------------------|----------|----------|------------|------------|------------|------------|------------|------------|----------|
| 7E  | R/W | RX FIFO Control      | Reserved | Reserved | rxafthr[5] | rxafthr[4] | rxafthr[3] | rxafthr[2] | rxafthr[1] | rxafthr[0] | 37h      |

Both the TX and RX FIFOs may be cleared or reset with the ffclrtx and ffclrrx bits in "Register 08h. Operating Mode and Function Control 2," on page 92. All interrupts may be enabled by setting the Interrupt Enabled bits in "Register 05h. Interrupt Enable 1" and "Register 06h. Interrupt Enable 2," on page 90. If the interrupts are not enabled the function will not generate an interrupt on the nIRQ pin but the bits will still be read correctly in the Interrupt Status registers.

## 6.2. Packet Configuration

When using the FIFOs, automatic packet handling may be enabled for TX mode, RX mode, or both. "Register 30h. Data Access Control" through "Register 4Bh. Received Packet Length," on page 127 control the configuration, status, and decoded RX packet data for Packet Handling. The usual fields for network communication (such as preamble, synchronization word, headers, packet length, and CRC) can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload greatly reduces the amount of communication between the microcontroller and the Si4431 and therefore also reduces the required computational power of the microcontroller.

The general packet structure is shown in Figure 17. The length of each field is shown below the field. The preamble pattern is always a series of alternating ones and zeroes, starting with a one. All the fields have programmable lengths to accommodate different applications. The most common CRC polynomials are available for selection.

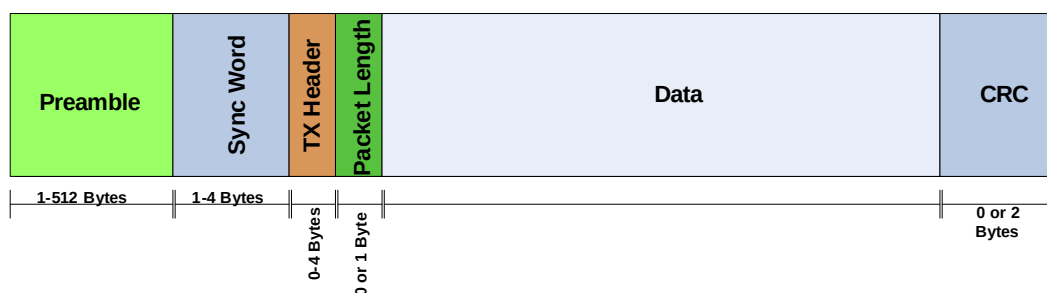


**Figure 17. Packet Structure**

An overview of the packet handler configuration registers is shown in Table 14. A complete register description can be found in "12.1. Complete Register Table and Descriptions".

6.3. Packet Handler TX Mode

If the TX packet length is set the packet handler will send the number of bytes in the packet length field before returning to ready mode and asserting the packet sent interrupt. To resume sending data from the FIFO the microcontroller needs to command the chip to re-enter TX mode Figure 18 provides an example transaction where the packet length is set to three bytes.

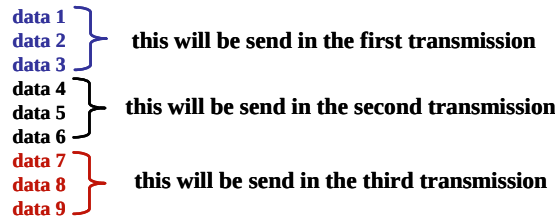


Figure 18. Multiple Packets in TX Packet Handler

6.4. Packet Handler RX Mode

6.4.1. Packet Handler Disabled

When the packet handler is disabled certain portions of the packet handler are still required. Proper modem operation requires preamble and sync, as shown in Figure 19. Bits after sync will be treated as raw data with no qualification. This mode allows for the creation of a custom packet handler when the automatic qualification parameters are not sufficient. Manchester encoding is supported but the use of data whitening, CRC, or header checks is not.

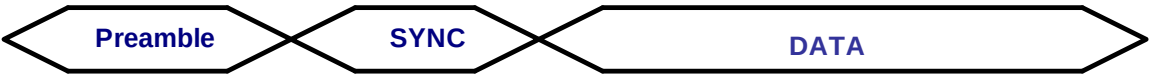


Figure 19. Required RX Packet Structure with Packet Handler Disabled

6.4.2. Packet Handler Enabled

When the packet handler is enabled, all the fields of the packet structure need to be configured. If multiple packets are desired to be stored in the FIFO, then there are options available for the different fields that will be stored into the FIFO. Figure 20 demonstrates the options and settings available when multiple packets are enabled. Figure 21 demonstrates the operation of fixed packet length and correct/incorrect packets.

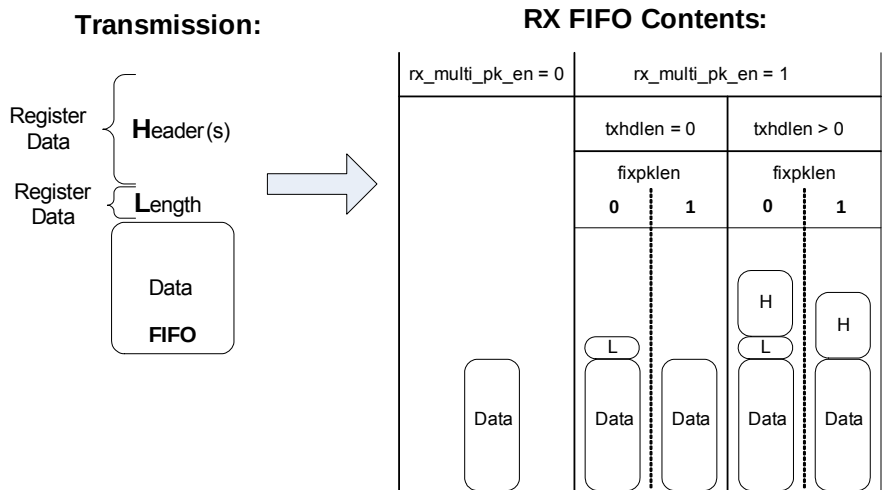


Figure 20. Multiple Packets in RX Packet Handler

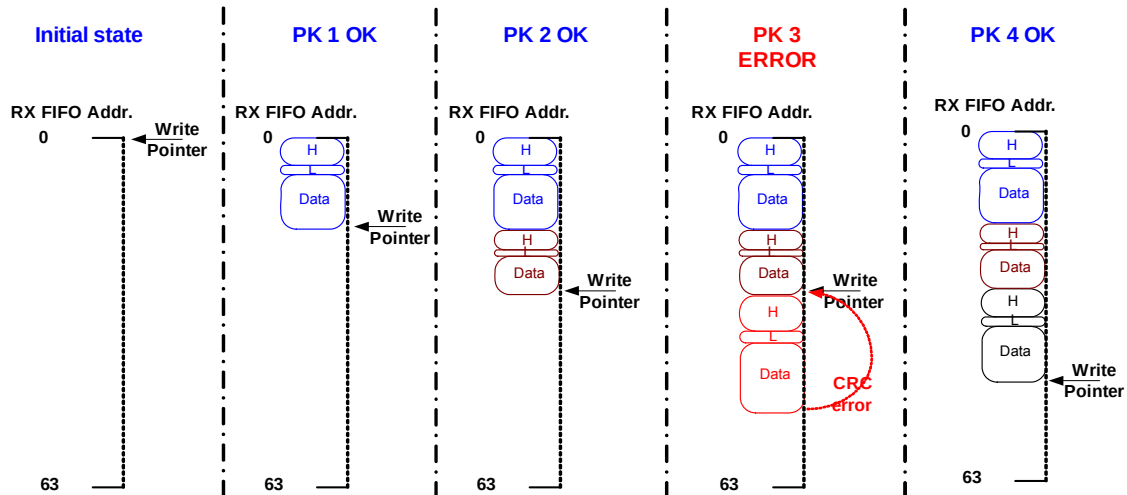


Figure 21. Multiple Packets in RX with CRC or Header Error

Table 13. RX Packet Handler Configuration

| Data modes | dtmod[1:0] | enpacrx | Direct Data and CLK IO | Preamble & Sync word detection | Header Handling | Data Storage in FIFO | CRC Handling | Manchester                  | Whitening |
|------------|------------|---------|------------------------|--------------------------------|-----------------|----------------------|--------------|-----------------------------|-----------|
| FIFO_PH    | 10         | 1       | option                 | set                            | option          | set                  | option       | option                      | Option    |
| FIFO       | 10         | 0       | option                 | set                            | —               | set                  | —            | option                      | —         |
| Direct     | 0X         | X       | set                    | set                            | —               | —                    | —            | Optional for sync-detection | —         |

Table 14. Packet Handler Registers

| Add | R/W | Function/Description       | D7         | D6         | D5         | D4         | D3         | D2          | D1          | D0         | POR Def. |
|-----|-----|----------------------------|------------|------------|------------|------------|------------|-------------|-------------|------------|----------|
| 30  | R/W | Data Access Control        | enpacrx    | lsbfrst    | crcdonly   | *          | enpactx    | encrc       | crc[1]      | crc[0]     | 1Dh      |
| 31  | R   | EzMAC status               | 0          | rxrcr1     | pksrcch    | pkrx       | pkvalid    | crccerror   | pktx        | pkscnt     | —        |
| 32  | R/W | Header Control 1           | bcen[3]    | enbcast[2] | enbcast[1] | enbcast[0] | hdch[3]    | hdch[2]     | hdch[1]     | hdch[0]    | 0Ch      |
| 33  | R/W | Header Control 2           | Reserved   | hdlen[2]   | hdlen[1]   | hdlen[0]   | fixpklen   | syncclen[1] | syncclen[0] | prealen[8] | 22h      |
| 34  | R/W | Preamble Length            | prealen[7] | prealen[6] | prealen[5] | prealen[4] | prealen[3] | prealen[2]  | prealen[1]  | prealen[0] | 07h      |
| 35  | R/W | Preamble Detection Control | preath[4]  | preath[3]  | preath[2]  | preath[1]  | preath[0]  | Reserved    | Reserved    | Reserved   | 20h      |
| 36  | R/W | Sync Word 3                | sync[31]   | sync[30]   | sync[29]   | sync[28]   | sync[27]   | sync[26]    | sync[25]    | sync[24]   | 2Dh      |
| 37  | R/W | Sync Word 2                | sync[23]   | sync[22]   | sync[21]   | sync[20]   | sync[19]   | sync[18]    | sync[17]    | sync[16]   | D4h      |
| 38  | R/W | Sync Word 1                | sync[15]   | sync[14]   | sync[13]   | sync[12]   | sync[11]   | sync[10]    | sync[9]     | sync[8]    | 00h      |
| 39  | R/W | Sync Word 0                | sync[7]    | sync[6]    | sync[5]    | sync[4]    | sync[3]    | sync[2]     | sync[1]     | sync[0]    | 00h      |
| 3A  | R/W | Transmit Header 3          | txhd[31]   | txhd[30]   | txhd[29]   | txhd[28]   | txhd[27]   | txhd[26]    | txhd[25]    | txhd[24]   | 00h      |
| 3B  | R/W | Transmit Header 2          | txhd[23]   | txhd[22]   | txhd[21]   | txhd[20]   | txhd[19]   | txhd[18]    | txhd[17]    | txhd[16]   | 00h      |
| 3C  | R/W | Transmit Header 1          | txhd[15]   | txhd[14]   | txhd[13]   | txhd[12]   | txhd[11]   | txhd[10]    | txhd[9]     | txhd[8]    | 00h      |
| 3D  | R/W | Transmit Header 0          | txhd[7]    | txhd[6]    | txhd[5]    | txhd[4]    | txhd[3]    | txhd[2]     | txhd[1]     | txhd[0]    | 00h      |
| 3E  | R/W | Transmit Packet Length     | pklen[7]   | pklen[6]   | pklen[5]   | pklen[4]   | pklen[3]   | pklen[2]    | pklen[1]    | pklen[0]   | 00h      |
| 3F  | R/W | Check Header 3             | chhd[31]   | chhd[30]   | chhd[29]   | chhd[28]   | chhd[27]   | chhd[26]    | chhd[25]    | chhd[24]   | 00h      |
| 40  | R/W | Check Header 2             | chhd[23]   | chhd[22]   | chhd[21]   | chhd[20]   | chhd[19]   | chhd[18]    | chhd[17]    | chhd[16]   | 00h      |
| 41  | R/W | Check Header 1             | chhd[15]   | chhd[14]   | chhd[13]   | chhd[12]   | chhd[11]   | chhd[10]    | chhd[9]     | chhd[8]    | 00h      |
| 42  | R/W | Check Header 0             | chhd[7]    | chhd[6]    | chhd[5]    | chhd[4]    | chhd[3]    | chhd[2]     | chhd[1]     | chhd[0]    | 00h      |
| 43  | R/W | Header Enable 3            | hden[31]   | hden[30]   | hden[29]   | hden[28]   | hden[27]   | hden[26]    | hden[25]    | hden[24]   | FFh      |
| 44  | R/W | Header Enable 2            | hden[23]   | hden[22]   | hden[21]   | hden[20]   | hden[19]   | hden[18]    | hden[17]    | hden[16]   | FFh      |
| 45  | R/W | Header Enable 1            | hden[15]   | hden[14]   | hden[13]   | hden[12]   | hden[11]   | hden[10]    | hden[9]     | hden[8]    | FFh      |
| 46  | R/W | Header Enable 0            | hden[7]    | hden[6]    | hden[5]    | hden[4]    | hden[3]    | hden[2]     | hden[1]     | hden[0]    | FFh      |
| 47  | R   | Received Header 3          | rxhd[31]   | rxhd[30]   | rxhd[29]   | rxhd[28]   | rxhd[27]   | rxhd[26]    | rxhd[25]    | rxhd[24]   | —        |
| 48  | R   | Received Header 2          | rxhd[23]   | rxhd[22]   | rxhd[21]   | rxhd[20]   | rxhd[19]   | rxhd[18]    | rxhd[17]    | rxhd[16]   | —        |
| 49  | R   | Received Header 1          | rxhd[15]   | rxhd[14]   | rxhd[13]   | rxhd[12]   | rxhd[11]   | rxhd[10]    | rxhd[9]     | rxhd[8]    | —        |
| 4A  | R   | Received Header 0          | rxhd[7]    | rxhd[6]    | rxhd[5]    | rxhd[4]    | rxhd[3]    | rxhd[2]     | rxhd[1]     | rxhd[0]    | —        |
| 4B  | R   | Received Packet Length     | rxplen[7]  | rxplen[6]  | rxplen[5]  | rxplen[4]  | rxplen[3]  | rxplen[2]   | rxplen[1]   | rxplen[0]  | —        |

## 6.5. Data Whitening, Manchester Encoding, and CRC

Data whitening can be used to avoid extended sequences of 0s or 1s in the transmitted data stream to achieve a more uniform spectrum. When enabled, the payload data bits are XORed with a pseudorandom sequence output from the built-in PN9 generator. The generator is initialized at the beginning of the payload. The receiver recovers the original data by repeating this operation. Manchester encoding can be used to ensure a dc-free transmission and good synchronization properties. When Manchester encoding is used, the effective datarate is unchanged but the actual datarate (preamble length, etc.) is doubled due to the nature of the encoding. The effective datarate when using Manchester encoding is **limited to 64 kbps**. Data Whitening and Manchester encoding can be selected with "Register 70h. Modulation Mode Control 1". The CRC is configured via "Register 30h. Data Access Control".

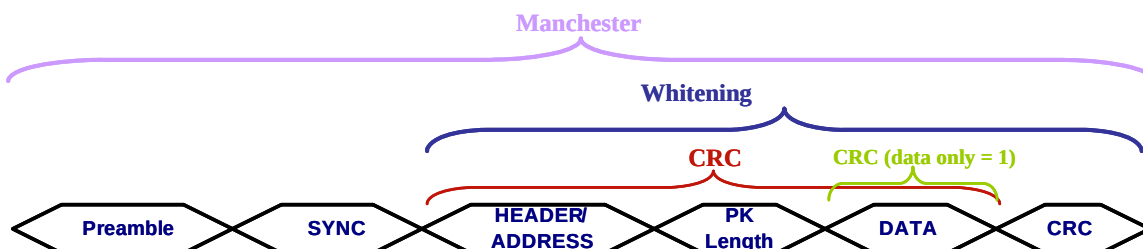


Figure 22. Operation of Data Whitening, Manchester Encoding, and CRC

## 6.6. Preamble Detector

The Si4431 has integrated automatic preamble detection. The preamble length is configurable from 1–256 bytes using the prealen[7:0] field in "Register 33h. Header Control 2" and "Register 34h. Preamble Length", as described in "6.2. Packet Configuration". The preamble detection threshold, preath[4:0] as set in "Register 35h. Preamble Detection Control 1", is in units of 4 bits. The preamble detector searches for a preamble pattern with a length of preath[4:0].

When a false preamble detect occurs, the receiver will continue searching for the preamble when no sync word is detected.

The Preamble Detector output may be programmed onto one of the GPIOs or read in the Interrupt Status registers.

## 6.7. Preamble Length

The required preamble length threshold will depend on when the receive mode is entered in relation to the transmitted packet. When the receiver is enabled long before the arrival of the packet, then a short preamble detection threshold might result in false detects on the received noise before the actual preamble arrives. In this case, it is recommended to program a 20 bit preamble detection threshold. A shorter Preamble Detection Threshold might be chosen when occasional false detects are tolerable. When antenna diversity is enabled, it is advised to use a 20 bit preamble detection threshold. When the receiver is synchronously enabled just before the start of the packet, then a shorter preamble detection threshold might be chosen (e.g., 8 bit).

The required preamble length is determined from the sum of the receiver settling time and the preamble detection threshold. The receiver settling time is listed in Table 15.

Table 15. Minimum Receiver Settling Time

| Mode                                           | Approximate receiver settling time | Recommended preamble length with 8-bit detection threshold | Recommended preamble length with 20-bit detection threshold |
|------------------------------------------------|------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|
| (G)FSK AFC Disabled                            | 1 byte                             | 20 bits                                                    | 32 bits                                                     |
| (G)FSK AFC Enabled                             | 2 byte                             | 28 bits                                                    | 40 bits                                                     |
| (G)FSK AFC Disabled +Antenna Diversity Enabled | 1 byte                             | —                                                          | 64 bits                                                     |
| (G)FSK AFC Enabled +Antenna Diversity Enabled  | 2 byte                             | —                                                          | 8 byte                                                      |
| OOK                                            | 2 byte                             | 3 byte                                                     | 4 byte                                                      |
| OOK + Antenna Diversity Enabled                | 8 byte                             | —                                                          | 8 byte                                                      |

**Note:** The recommended preamble length and the preamble detection threshold may be shortened when occasional packet errors are tolerable.

## 6.8. Invalid Preamble Detector

When scanning channels in a Frequency Hopping System, it is desirable to determine if a channel is valid in the minimum amount of time. The preamble detector can output an invalid preamble detect signal. When an error is detected in the preamble, the Invalid Preamble Detect signal (nPQD) is asserted, indicating an invalid channel. The signal can be used to qualify the channel without requiring the full preamble to be received. The Preamble Detect and Invalid Preamble Detect signals are available in "Register 03h. Interrupt/Status 1" and "Register 04h. Interrupt/Status 2," on page 87.

The Invalid Preamble Detector issues an interrupt when no valid preamble signal is found. After the receiver is enabled, the Invalid Preamble Detector will be held low for 16 Tb (Tb is the time of the bit duration) to allow the receiver to settle. The 16 Tb is a fixed time which will work with a 4-byte Preamble (or longer) when AFC is enabled, or a 3-byte preamble (or longer) when AFC is disabled. The invalid preamble detect interrupt can be useful to save power and speed-up search in receive mode.

It is advised to disable the invalid preamble interrupt when Antenna Diversity is enabled. The Invalid Preamble Detect interrupt may be triggered during the Antenna Diversity algorithm if one of the antennas is weak but the other is capable of still receiving the signal if the Antenna Diversity algorithm is allowed to complete.

## 6.9. TX Retransmission and Auto TX

The Si4431 is capable of automatically retransmitting the last packet in the FIFO if no additional packets were loaded into the TX FIFO. Automatic Retransmission is achieved by entering the TX state with the txon bit set. This feature is useful for Beacon transmission or when retransmission is required due to the absence of a valid acknowledgement. Only packets that fit completely in the TX FIFO are valid for retransmit. When it is necessary to transmit longer packets, the TX FIFO uses the circular read/write capability.

An Automatic Transmission is also available. When autotx = 1 the transceiver will enter automatically TX State when the TX FIFO is almost full. When the packet is sent, the transceiver will automatically return to the IDLE State.

| Add | R/W | Function/Description           | D7        | D6        | D5        | D4    | D3     | D2    | D1      | D0      | POR Def. |
|-----|-----|--------------------------------|-----------|-----------|-----------|-------|--------|-------|---------|---------|----------|
| 08  | R/W | Operating & Function Control 2 | antdiv[2] | antdiv[1] | antdiv[0] | rxmpk | autotx | enldm | ffclrrx | ffclrtx | 00h      |

## 7. RX Modem Configuration

### 7.1. Modem Settings for FSK and GFSK

The modem performs channel selection and demodulation in the digital domain. The channel filter bandwidth is configurable from 620 to 2.6 kHz. The data-rate, modulation index, and bandwidth are set via registers 1C–25. The modulation index is equal to 2 times the peak deviation divided by the data rate (Rb).

Table 16 gives the modem register settings for various common data-rates. Select the desired data-rate (Rb), and Deviation (Fd) to determine the proper register settings. For data-rates and modulation types not listed in the table a calculator tool within WDS can be used.

When Manchester coding is disabled, the required channel filter bandwidth is calculated as  $BW = 2 \times (Fd + 0.25Rb)$  where Fd is the frequency deviation and Rb is the data rate. For modulation indices below 1 the required channel filter bandwidth is calculated as  $BW = Fd + Rb$ . The channel filter needs to be increased when the frequency offset between transmitter and receiver is more than half the channel filter bandwidth. In this case it is recommended to enable the AFC and choose the IF bandwidth equal to 2 x frequency offset.

**Table 16. RX Modem Configurations for FSK and GFSK**

| RX Modem setting examples for GFSK and FSK |      |           |         |                       |               |             |             |             |              |
|--------------------------------------------|------|-----------|---------|-----------------------|---------------|-------------|-------------|-------------|--------------|
| Application parameters                     |      |           |         | Register values (hex) |               |             |             |             |              |
| Rb                                         | Fd   | mod index | BW -3dB | dwn3_bypass           | ndec_exp[2:0] | filset[3:0] | rxosr[10:0] | ncoff[19:0] | crgain[10:0] |
| kbps                                       | kHz  |           | kHz     | 1Ch                   | 1Ch           | 1Ch         | 20,21h      | 21,22,23h   | 24,25h       |
| 2                                          | 5    | 5.00      | 11.5    | 0                     | 3             | 3           | 0FA         | 08312       | 06B          |
| 2.4                                        | 4.8  | 4.00      | 11.5    | 0                     | 3             | 3           | 0D0         | 09D49       | 0A0          |
| 2.4                                        | 36   | 30.00     | 75.2    | 0                     | 0             | 1           | 683         | 013A9       | 005          |
| 4.8                                        | 4.8  | 2.00      | 12.1    | 0                     | 3             | 4           | 068         | 13A93       | 278          |
| 4.8                                        | 45   | 18.75     | 95.3    | 0                     | 0             | 4           | 341         | 02752       | 00A          |
| 9.6                                        | 4.8  | 1.00      | 18.9    | 0                     | 2             | 1           | 068         | 13A93       | 4EE          |
| 9.6                                        | 45   | 9.38      | 95.3    | 0                     | 0             | 4           | 1A1         | 04EA5       | 024          |
| 10                                         | 5    | 1.00      | 18.9    | 0                     | 2             | 1           | 064         | 147AE       | 521          |
| 10                                         | 40   | 8.00      | 90      | 0                     | 0             | 3           | 190         | 051EC       | 02B          |
| 19.2                                       | 9.6  | 1.00      | 37.7    | 0                     | 1             | 1           | 068         | 13A93       | 4EE          |
| 20                                         | 10   | 1.00      | 37.7    | 0                     | 1             | 1           | 064         | 147AE       | 521          |
| 20                                         | 40   | 4.00      | 95.3    | 0                     | 0             | 4           | 0C8         | 0A3D7       | 0A6          |
| 38.4                                       | 19.6 | 1.02      | 75.2    | 0                     | 0             | 1           | 068         | 13A93       | 4D5          |
| 40                                         | 20   | 1.00      | 75.2    | 0                     | 0             | 1           | 064         | 147AE       | 521          |
| 40                                         | 40   | 2.00      | 112.1   | 0                     | 0             | 5           | 064         | 147AE       | 291          |
| 50                                         | 25   | 1.00      | 75.2    | 0                     | 0             | 1           | 050         | 1999A       | 668          |
| 57.6                                       | 28.8 | 1.00      | 90      | 0                     | 0             | 3           | 045         | 1D7DC       | 76E          |
| 100                                        | 50   | 1.00      | 191.5   | 1                     | 0             | F           | 078         | 11111       | 446          |
| 100                                        | 300  | 6.00      | 620.7   | 1                     | 0             | E           | 078         | 11111       | 0B8          |
| 125                                        | 125  | 2.00      | 335.5   | 1                     | 0             | 8           | 060         | 15555       | 2AD          |

## 7.1.1. Advanced FSK and GFSK Settings

In nearly all cases, the information in Table 16, “RX Modem Configurations for FSK and GFSK,” on page 49 can be used to determine the required FSK and GFSK modem parameters. The section includes a more detailed discussion of the various modem parameters to allow for experienced designers to further configure the modem performance.

In FSK or GFSK mode the receiver can handle a wide range of modulation indices ranging from 0.5 up to 32. The modulation index ( $h$ ) is defined by the following:

$$h = \frac{2 \times Fd}{Rb \times (1 + enmanch)}$$

When the modulation index is 1 or higher the modulation bandwidth can be approximated by the following equation:

$$BW_{mod} = \left( \frac{Rb}{2} \times (1 + enmanch) + 2 \times Fd \right)$$

When the modulation index is lower than 1 the modulation bandwidth can be approximated by the following:

$$BW_{mod} = (Rb \times (1 + enmanch) + Fd)$$

Where  $BW_{mod}$  is an approximation of the modulation bandwidth in kHz,  $Rb$  is the payload bit rate in kbps,  $Fd$  is the frequency deviation of the received GFSK/FSK signal in kHz and  $enmanch$  is the Manchester Coding parameter (see Reg. 70h,  $enmach$  is 1 when Manchester coding is enabled,  $enmanch$  is 0 when disabled).

The bandwidth of the channel select filter in the receiver might need some extra bandwidth to cope with tolerances in transmit and receive frequencies which depends on the tolerances of the applied crystals. When the relative frequency error ( $F_{error}$ ) between transmitter and receiver is less than half the modulation bandwidth ( $BW_{mod}$ ) then the AFC will correct the frequency error without needing extra bandwidth. When the frequency error exceeds  $BW_{mod}/2$  then some extra bandwidth will be needed to assure proper AFC operation under worst case conditions. When the AFC is enabled it is recommended to set the bandwidth of the channel select filter ( $BW_{ch-sel}$ ) according to the formulas below:

$$F_{error} \leq \frac{BW_{mod}}{2} \Rightarrow BW_{ch-sel} = BW_{mod}$$
$$F_{error} > \frac{BW_{mod}}{2} \Rightarrow BW_{ch-sel} = 2 \times F_{error}$$

When the AFC is disabled it is recommended to set the bandwidth of the channel select filter ( $BW_{ch-sel}$ ) according to the following:

$$BW_{ch-sel} = BW_{mod} + 2 \times F_{error}$$

When the required bandwidth (BW) is calculated then the three filter parameters,  $ndec\_exp$ ,  $dwn3\_bypass$  and  $filset$ , can be found from the table below. When the calculated bandwidth value is not exactly available then select the higher available bandwidth closest to the calculated bandwidth.

Table 17. Filter Bandwidth Parameters

| BW [kHz] | ndec_exp<br>1C-[6:4] | dwn3_bypass<br>1C-[7] | filset<br>1C-[3:0] | BW [kHz] | ndec_exp<br>1C-[6:4] | dwn3_bypass<br>1C-[7] | filset<br>1C-[3:0] |
|----------|----------------------|-----------------------|--------------------|----------|----------------------|-----------------------|--------------------|
| 2.6      | 5                    | 0                     | 1                  | 41.7     | 1                    | 0                     | 2                  |
| 2.8      | 5                    | 0                     | 2                  | 45.2     | 1                    | 0                     | 3                  |
| 3.1      | 5                    | 0                     | 3                  | 47.9     | 1                    | 0                     | 4                  |
| 3.2      | 5                    | 0                     | 4                  | 56.2     | 1                    | 0                     | 5                  |
| 3.7      | 5                    | 0                     | 5                  | 64.1     | 1                    | 0                     | 6                  |
| 4.2      | 5                    | 0                     | 6                  | 69.2     | 1                    | 0                     | 7                  |
| 4.5      | 5                    | 0                     | 7                  | 75.2     | 0                    | 0                     | 1                  |
| 4.9      | 4                    | 0                     | 1                  | 83.2     | 0                    | 0                     | 2                  |
| 5.4      | 4                    | 0                     | 2                  | 90.0     | 0                    | 0                     | 3                  |
| 5.9      | 4                    | 0                     | 3                  | 95.3     | 0                    | 0                     | 4                  |
| 6.1      | 4                    | 0                     | 4                  | 112.1    | 0                    | 0                     | 5                  |
| 7.2      | 4                    | 0                     | 5                  | 127.9    | 0                    | 0                     | 6                  |
| 8.2      | 4                    | 0                     | 6                  | 137.9    | 0                    | 0                     | 7                  |
| 8.8      | 4                    | 0                     | 7                  | 142.8    | 1                    | 1                     | 4                  |
| 9.5      | 3                    | 0                     | 1                  | 167.8    | 1                    | 1                     | 5                  |
| 10.6     | 3                    | 0                     | 2                  | 181.1    | 1                    | 1                     | 9                  |
| 11.5     | 3                    | 0                     | 3                  | 191.5    | 0                    | 1                     | 15                 |
| 12.1     | 3                    | 0                     | 4                  | 225.1    | 0                    | 1                     | 1                  |
| 14.2     | 3                    | 0                     | 5                  | 248.8    | 0                    | 1                     | 2                  |
| 16.2     | 3                    | 0                     | 6                  | 269.3    | 0                    | 1                     | 3                  |
| 17.5     | 3                    | 0                     | 7                  | 284.9    | 0                    | 1                     | 4                  |
| 18.9     | 2                    | 0                     | 1                  | 335.5    | 0                    | 1                     | 8                  |
| 21.0     | 2                    | 0                     | 2                  | 361.8    | 0                    | 1                     | 9                  |
| 22.7     | 2                    | 0                     | 3                  | 420.2    | 0                    | 1                     | 10                 |
| 24.0     | 2                    | 0                     | 4                  | 468.4    | 0                    | 1                     | 11                 |
| 28.2     | 2                    | 0                     | 5                  | 518.8    | 0                    | 1                     | 12                 |
| 32.2     | 2                    | 0                     | 6                  | 577.0    | 0                    | 1                     | 13                 |
| 34.7     | 2                    | 0                     | 7                  | 620.7    | 0                    | 1                     | 14                 |
| 37.7     | 1                    | 0                     | 1                  |          |                      |                       |                    |

## 7.2. Modem Settings for OOK

The Si4431 is configured for OOK mode by setting the modtyp[1:0] field to OOK in "Register 71h. Modulation Mode Control 2". In OOK mode, the following parameters can be configured: data rate, manchester coding, channel filter bandwidth, and the clock recovery oversampling rate.

The required data rate (Rb) is configured via the txdr[15:0] field in "Register 6Eh. TX Data Rate 1" and "Register 6Fh. TX Data Rate 0". For data rates  $\leq 30$  kbps, "txdtrscale" in "Register 70h. Modulation Mode Control 1" should be set to 1 for increased data rate precision. Manchester coding is enabled by setting enmanch in Register 70h.

The receive channel select filter bandwidth is configured via "Register 1Ch. IF Filter Bandwidth". The register settings for the available channel bandwidths are shown in Table 18.

**Table 18. Channel Filter Bandwidth Settings**

| BW[kHz] | dwn3_bypass | filset[3:0] |
|---------|-------------|-------------|
| 75.2    | 0           | 1           |
| 83.2    | 0           | 2           |
| 90      | 0           | 3           |
| 95.3    | 0           | 4           |
| 112.1   | 0           | 5           |
| 127.9   | 0           | 6           |
| 137.9   | 0           | 7           |
| 191.5   | 1           | F           |
| 225.1   | 1           | 1           |
| 248.8   | 1           | 2           |
| 269.3   | 1           | 3           |
| 284.9   | 1           | 4           |
| 335.5   | 1           | 8           |
| 361.8   | 1           | 9           |
| 420.2   | 1           | 10          |
| 468.4   | 1           | 11          |
| 518.8   | 1           | 12          |
| 577     | 1           | 13          |
| 620.7   | 1           | 14          |

The proper settings for ndec[2:0] are listed in Table 19 where Rb is the data rate (Rb) which is doubled when Manchester coding is enabled.

Table 19. ndec[2:0] Settings

| Rb(1+ enmanch) [kbps] |     | ndec[2:0] |
|-----------------------|-----|-----------|
| Min                   | Max |           |
| 0                     | 1   | 5         |
| 1                     | 2   | 4         |
| 2                     | 3   | 3         |
| 3                     | 8   | 2         |
| 8                     | 40  | 1         |
| 40                    | 65  | 0         |

The clock recovery oversampling rate is set via rxosr[10:0] in "Register 20h. Clock Recovery Oversampling Rate" and "Register 21h. Clock Recovery Offset 2".

ndec\_exp and dwn3\_bypass together with the receive data rate (Rb) are used to calculate rxosr:

$$rxosr = \frac{500 \times (1 + 2 \times dwn3\_bypass)}{2^{ndec\_exp-3} \times Rb \times (1 + enmanch)}$$

Where: Rb is in kbps and enmanch is the Manchester Coding parameter. The resulting rxosr[10:0] value should be rounded to an integer hexadecimal number.

The clock recovery offset ncoff[19:0] in "Register 21h. Clock Recovery Offset 2", "Register 22h. Clock Recovery Offset 1", and "Register 23h. Clock Recovery Offset 0" is calculated as follows:

$$ncoff = \frac{Rb \times (1 + enmanch) \times 2^{20+ndec\_exp}}{500 \times (1 + 2 \times dwn3\_bypass)}$$

Where: Rb is in kbps.

The clock recovery gain crgain[10:0] in "Register 24h. Clock Recovery Timing Loop Gain 1" and "Register 25h. Clock Recovery Timing Loop Gain 0" is calculated as follows:

$$crgain = 2 + \frac{2^{16}}{rxosr}$$

Table 20. RX Modem Configuration for OOK with Manchester Disabled

| RX Modem Setting Examples for OOK (Manchester Disabled) |       |                 |               |             |             |             |              |
|---------------------------------------------------------|-------|-----------------|---------------|-------------|-------------|-------------|--------------|
| Appl Parameters                                         |       | Register Values |               |             |             |             |              |
| Rb                                                      | RX BW | dwn3_bypass     | ndec_exp[2:0] | filset[3:0] | rxosr[10:0] | ncoff[19:0] | crgain[10:0] |
| [kbps]                                                  | [kHz] | 1Ch             | 1Ch           | 1Ch         | 20,21h      | 21,22,23h   | 24,25h       |
| 1.2                                                     | 75    | 0               | 4             | 1           | 0D0         | 09D49       | 13D          |
| 1.2                                                     | 110   | 0               | 4             | 5           | 0D0         | 09D49       | 13D          |
| 1.2                                                     | 335   | 1               | 4             | 8           | 271         | 0346E       | 06B          |
| 1.2                                                     | 420   | 1               | 4             | A           | 271         | 0346E       | 06B          |
| 1.2                                                     | 620   | 1               | 4             | E           | 271         | 0346E       | 06B          |
| 2.4                                                     | 335   | 1               | 3             | 8           | 271         | 0346E       | 06B          |
| 4.8                                                     | 335   | 1               | 2             | 8           | 271         | 0346E       | 06B          |
| 9.6                                                     | 335   | 1               | 1             | 8           | 271         | 0346E       | 06B          |
| 10                                                      | 335   | 1               | 1             | 8           | 258         | 0369D       | 06F          |
| 15                                                      | 335   | 1               | 1             | 8           | 190         | 051EC       | 0A6          |
| 19.2                                                    | 335   | 1               | 1             | 8           | 139         | 068DC       | 0D3          |
| 20                                                      | 335   | 1               | 1             | 8           | 12C         | 06D3A       | 0DC          |
| 30                                                      | 335   | 1               | 1             | 8           | 0C8         | 0A3D7       | 14A          |
| 38.4                                                    | 335   | 1               | 1             | 8           | 09C         | 0D1B7       | 1A6          |
| 40                                                      | 335   | 1               | 1             | 8           | 096         | 0DA74       | 1B7          |

Table 21. RX Modem Configuration for OOK with Manchester Enabled

| RX Modem Setting Examples for OOK (Manchester Enabled) |       |                 |               |             |             |             |              |
|--------------------------------------------------------|-------|-----------------|---------------|-------------|-------------|-------------|--------------|
| Appl Parameters                                        |       | Register Values |               |             |             |             |              |
| Rb                                                     | RX BW | dwn3_bypass     | ndec_exp[2:0] | filset[3:0] | rxosr[10:0] | ncoff[19:0] | crgain[10:0] |
| [kbps]                                                 | [kHz] | 1Ch             | 1Ch           | 1Ch         | 20,21h      | 21,22,23h   | 24,25h       |
| 1.2                                                    | 75    | 0               | 3             | 1           | 0D0         | 04EA5       | 13D          |
| 1.2                                                    | 110   | 0               | 3             | 5           | 0D0         | 04EA5       | 13D          |
| 1.2                                                    | 335   | 1               | 3             | 8           | 271         | 01A37       | 06B          |
| 1.2                                                    | 420   | 1               | 3             | A           | 271         | 01A37       | 06B          |
| 1.2                                                    | 620   | 1               | 3             | E           | 271         | 01A37       | 06B          |
| 2.4                                                    | 335   | 1               | 2             | 8           | 271         | 01A37       | 06B          |
| 4.8                                                    | 335   | 1               | 1             | 8           | 271         | 01A37       | 06B          |
| 9.6                                                    | 335   | 1               | 1             | 8           | 139         | 0346E       | 0D3          |
| 10                                                     | 335   | 1               | 1             | 8           | 12C         | 0369D       | 0DC          |
| 15                                                     | 335   | 1               | 1             | 8           | 0C8         | 051EC       | 14A          |
| 19.2                                                   | 335   | 1               | 1             | 8           | 09C         | 068DC       | 1A6          |
| 20                                                     | 335   | 1               | 1             | 8           | 096         | 06D3A       | 1B7          |
| 30                                                     | 335   | 1               | 0             | 8           | 0C8         | 051EC       | 14A          |
| 38.4                                                   | 335   | 1               | 0             | 8           | 09C         | 068DC       | 1A6          |
| 40                                                     | 335   | 1               | 0             | 8           | 096         | 06D3A       | 1B7          |

## 8. Auxiliary Functions

### 8.1. Smart Reset

The Si4431 contains an enhanced integrated SMART RESET or POR circuit. The POR circuit contains both a classic level threshold reset as well as a slope detector POR. This reset circuit was designed to produce reliable reset signal in any circumstances. Reset will be initiated if any of the following conditions occur:

- Initial power on, when VDD starts from 0V: reset is active till VDD reaches  $V_{RR}$  (see table);
- When VDD decreases below  $V_{LD}$  for any reason: reset is active till VDD reaches  $V_{RR}$  again;
- A software reset via “Register 08h. Operating Mode and Function Control 2,” on page 92: reset is active for time  $T_{SWRST}$
- On the rising edge of a VDD glitch when the supply voltage exceeds the following time functioned limit:

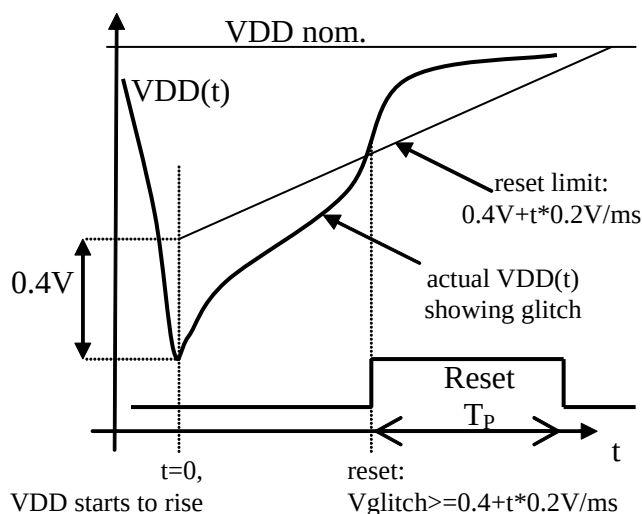


Figure 23. POR Glitch Parameters

Table 22. POR Parameters

| Parameter              | Symbol | Comment                                     | Min  | Typ | Max  | Unit |
|------------------------|--------|---------------------------------------------|------|-----|------|------|
| Release Reset Voltage  | VRR    |                                             | 0.85 | 1.3 | 1.75 | V    |
| Power-On VDD Slope     | SVDD   | tested VDD slope region                     | 0.03 |     | 300  | V/ms |
| Low VDD Limit          | VLD    | $VLD < VRR$ is guaranteed                   | 0.7  | 1   | 1.3  | V    |
| Software Reset Pulse   | TSWRST |                                             | 50   |     | 470  | us   |
| Threshold Voltage      | VTSD   |                                             |      | 0.4 |      | V    |
| Reference Slope        | k      |                                             |      | 0.2 |      | V/ms |
| VDD Glitch Reset Pulse | TP     | Also occurs after SDN, and initial power on | 5    | 15  | 40   | ms   |

The reset will initialize all registers to their default values. The reset signal is also available for output and use by the microcontroller by using the default setting for GPIO\_0. The inverted reset signal is available by default on GPIO\_1.

## 8.2. Microcontroller Clock

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through GPIO2. This feature is useful to lower BOM cost by using only one crystal in the system. The system clock frequency is selectable from one of 8 options, as shown below. Except for the 32.768 kHz option, all other frequencies are derived by dividing the Crystal Oscillator frequency. The 32.768 kHz clock signal is derived from an internal RC Oscillator or an external 32 kHz Crystal, depending on which is selected. The GPIO2 default is the microcontroller clock with a 1 MHz microcontroller clock output.

| Add | R/W | Function/Description         | D7 | D6 | D5      | D4      | D3    | D2      | D1      | D0      | POR Def. |
|-----|-----|------------------------------|----|----|---------|---------|-------|---------|---------|---------|----------|
| 0A  | R/W | Microcontroller Output Clock |    |    | clkt[1] | clkt[0] | enlfc | mclk[2] | mclk[1] | mclk[0] | 0Bh      |

| mclk[2:0] | Modulation Source |
|-----------|-------------------|
| 000       | 30 MHz            |
| 001       | 15 MHz            |
| 010       | 10 MHz            |
| 011       | 4 MHz             |
| 100       | 3 MHz             |
| 101       | 2 MHz             |
| 110       | 1 MHz             |
| 111       | 32.768 kHz        |

If the microcontroller clock option is being used there may be the need of a System Clock for the microcontroller while the Si4431 is in SLEEP mode. Since the Crystal Oscillator is disabled in SLEEP mode in order to save current, the low-power 32.768 kHz clock can be automatically switched to become the microcontroller clock. This feature is called Enable Low Frequency Clock and is enabled by the enlfc bit. When enlfc = 1 and the chip is in SLEEP mode then the 32.768 kHz clock will be provided to the microcontroller as the System Clock, regardless of the setting of mclk[2:0]. For example, if mclk[2:0] = 000, 30 MHz will be provided through the GPIO output pin to the microcontroller as the System Clock in all IDLE, TX, or RX states. When the chip is commanded to SLEEP mode, the System Clock will become 32.768 kHz.

Another available feature for the microcontroller clock is the Clock Tail, clkt[1:0]. If the Enable Low Frequency Clock feature is not enabled (enlfc = 0), then the System Clock to the microcontroller is disabled in SLEEP mode. However, it may be useful to provide a few extra cycles for the microcontroller to complete its operation prior to the shutdown of the System Clock signal. Setting the clkt[1:0] field will provide additional cycles of the System Clock before it shuts off.

| clkt[1:0] | Modulation Source |
|-----------|-------------------|
| 00        | 0 cycles          |
| 01        | 128 cycles        |
| 10        | 256 cycles        |
| 11        | 512 cycles        |

If an interrupt is triggered, the microcontroller clock will remain enabled regardless of the selected mode. As soon as the interrupt is read the state machine will then move to the selected mode. For instance, if the chip is commanded to Sleep mode but an interrupt has occurred the 30 MHz XTAL will not disable until the interrupt has been cleared.

### 8.3. General Purpose ADC

An 8-bit SAR ADC is integrated onto the chip for general purpose use, as well as for digitizing the temperature sensor reading. "Register 0Fh. ADC Configuration," on page 99 must be configured depending on the use of the GP ADC before use. The architecture of the ADC is demonstrated in Figure 24. First the input of the ADC must be selected by setting the ADCSEL[2:0] depending on the use of the ADC. For instance, if the ADC is going to be used to read out the internal temperature sensor, then ADCSEL[2:0] should be set to 000. Next, the input reference voltage to the ADC must be chosen. By default, the ADC uses the bandgap voltage as a reference so the input range of the ADC is from 0–1.02 V with an LSB resolution of 4 mV (1.02/255). Changing the ADC reference will change the LSB resolution accordingly.

Every time the ADC conversion is desired, the ADCStart bit in "Register 0Fh. ADC Configuration," on page 99 must be set to 1. This is a self clearing bit that will be cleared at the end of the conversion cycle of the ADC. The conversion time for the ADC is 350  $\mu$ s. After the 350  $\mu$ s or when the ADCstart/busy bit is cleared, then the ADC value may be read out of "Register 11h. ADC Value". Setting the "Register 10h. ADC Sensor Amplifier Offset", ADC Sensor Amplifier Offset is only necessary when the ADC is configured to used as a Bridge Sensor as described in the following section.

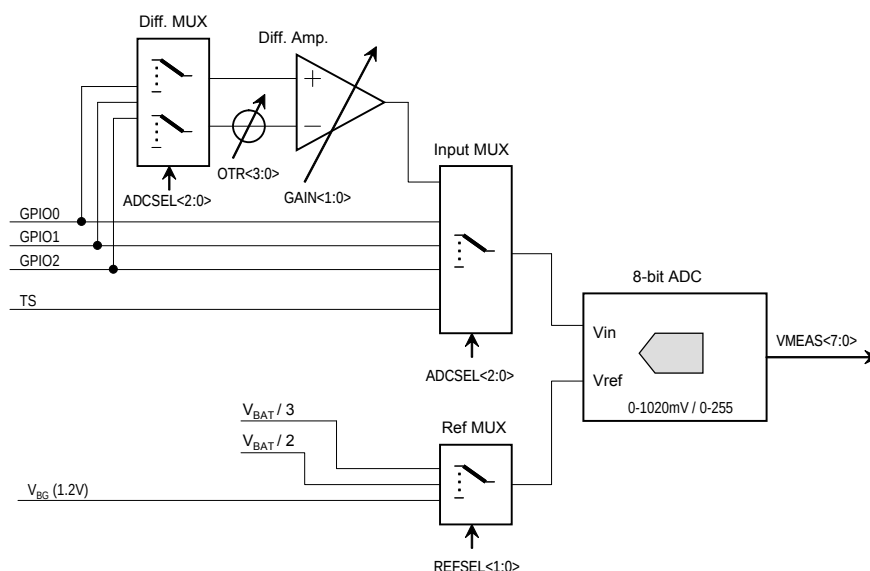


Figure 24. General Purpose ADC Architecture

| Add | R/W | Function/Description        | D7               | D6       | D5       | D4       | D3         | D2         | D1         | D0         | POR Def. |
|-----|-----|-----------------------------|------------------|----------|----------|----------|------------|------------|------------|------------|----------|
| 0F  | R/W | ADC Configuration           | adcstart/adcbusy | adcse[2] | adcse[1] | adcse[0] | adcref[1]  | adcref[0]  | adcgain[1] | adcgain[0] | 00h      |
| 10  | R/W | ADC Sensor Amplifier Offset |                  |          |          |          | adcoffs[3] | adcoffs[2] | adcoffs[1] | adcoffs[0] | 00h      |
| 11  | R   | ADC Value                   | adc[7]           | adc[6]   | adc[5]   | adc[4]   | adc[3]     | adc[2]     | adc[1]     | adc[0]     | —        |

8.3.1. ADC Differential Input Mode—Bridge Sensor Example

The differential input mode of ADC8 is designed to directly interface any bridge-type sensor, which is demonstrated in the figure below. As seen in the figure the use of the ADC in this configuration will utilize two GPIO pins. The supply source of the bridge and chip should be the same to eliminate the measuring error caused by battery discharging. For proper operation one of the VDD dependent references (VDD/2 or VDD/3) should be selected for the reference voltage of ADC8. VDD/2 reference should be selected for VDD lower than 2.7 V, VDD/3 reference should be selected for VDD higher than 2.7 V. The differential input mode supports programmable gain to match the input range of ADC8 to the characteristic of the sensor and VDD proportional programmable offset adjustment to compensate the offset of the sensor.

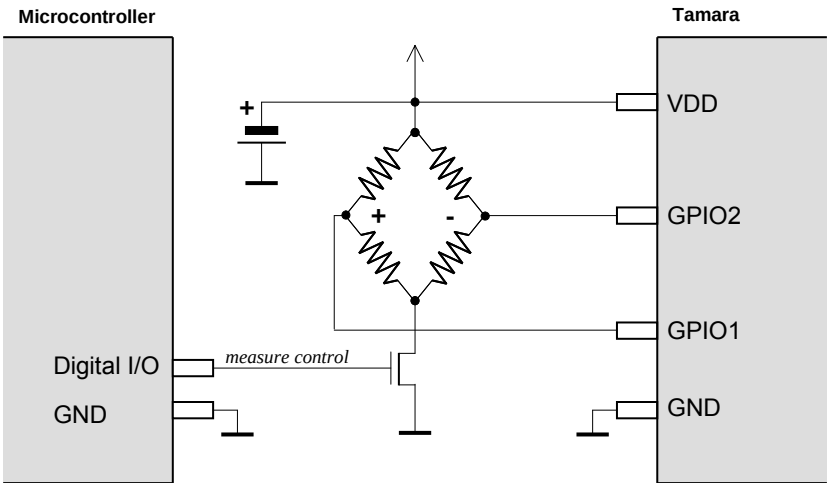


Figure 25. ADC Differential Input Example—Bridge Sensor

The `adcgain[1:0]` bits in "Register 0Eh. I/O Port Configuration" determine the gain of the differential/single ended amplifier. This is used to fit the input range of the ADC8 to bridge sensors having different sensitivity:

| adcgain[1] | adcgain[0] | Differential Gain |               | Input Range (% of VDD) |
|------------|------------|-------------------|---------------|------------------------|
|            |            | adcref[0] = 0     | adcref[0] = 1 |                        |
| 0          | 0          | 22/13             | 33/13         | 16.7                   |
| 0          | 1          | 44/13             | 66/13         | 8.4                    |
| 1          | 0          | 66/13             | 99/13         | 5.6                    |
| 1          | 1          | 88/13             | 132/13        | 4.2                    |

**Note:** The input range is the differential voltage measured between the selected GPIO pins corresponding to the full ADC range (255).  
The gain is different for different VDD dependent references so the reference change has no influence on input range and digital measured values.

The differential offset can be coarse compensated by the `adcoffs[3:0]` bits found in "Register 11h. ADC Value". Fine compensation should be done by the microcontroller software. The main reason for the offset compensation is to shift the negative offset voltage of the bridge sensor to the positive differential voltage range. This is essential as the differential input mode is unipolar. The offset compensation is VDD proportional, so the VDD change has no influence on the measured value.

| <code>adcoffs[3]</code> | Input Offset (% of VDD)                  |
|-------------------------|------------------------------------------|
| 0                       | 0 if <code>adcoffs[2:0] = 0</code>       |
|                         | $-(8 - \text{adcoffs}[2:0]) \times 0.12$ |
| 1                       | $\text{adcoffs}[2:0] \times 0.12$        |

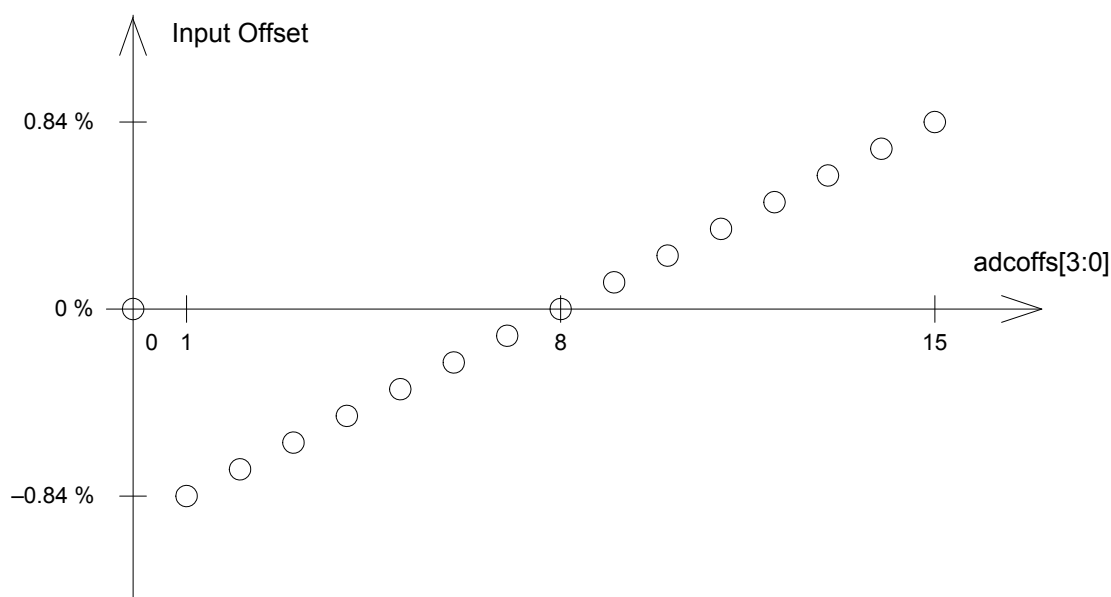


Figure 26. ADC Differential Input Offset for Sensor Offset Coarse Compensation

## 8.4. Temperature Sensor

An analog temperature sensor is integrated into the chip. The temperature sensor will be automatically enabled when the temperature sensor is selected as the input of the ADC or when the analog temp voltage is selected on the analog test bus. The temperature sensor value may be digitized using the general-purpose ADC and read out over the SPI through "Register 10h. ADC Sensor Amplifier Offset". The range of the temperature sensor is selectable to configure to the desired application and performance. The table below demonstrates the settings for the different temperature ranges and performance.

To use the Temp Sensor:

1. Set input for ADC to be Temperature Sensor, "Register 0Fh. ADC Configuration"—`adcse[2:0] = 000`
2. Set Reference for ADC, "Register 0Fh. ADC Configuration"—`adcref[1:0] = 00`
3. Set Temperature Range for ADC, "Register 12h. Temperature Sensor Calibration"—`tsrange[1:0]`
4. Set `entsoffs = 1`, "Register 12h. Temperature Sensor Calibration"
5. Trigger ADC Reading, "Register 0Fh. ADC Configuration"—`adcstart = 1`
6. Read-out Value—Read Address in "Register 11h. ADC Value"

| Add | R/W | Function/Description       | D7                      | D6                      | D5                     | D4                     | D3                       | D2                       | D1                       | D0                       | POR Def. |
|-----|-----|----------------------------|-------------------------|-------------------------|------------------------|------------------------|--------------------------|--------------------------|--------------------------|--------------------------|----------|
| 12  | R/W | Temperature Sensor Control | <code>tsrange[1]</code> | <code>tsrange[0]</code> | <code>entsoffs</code>  | <code>entstrim</code>  | <code>vbgttrim[3]</code> | <code>vbgttrim[2]</code> | <code>vbgttrim[1]</code> | <code>vbgttrim[0]</code> | 20h      |
| 13  | R/W | Temperature Value Offset   | <code>tvoffs[7]</code>  | <code>tvoffs[6]</code>  | <code>tvoffs[5]</code> | <code>tvoffs[4]</code> | <code>tvoffs[3]</code>   | <code>tvoffs[2]</code>   | <code>tvoffs[1]</code>   | <code>tvoffs[0]</code>   | 00h      |

**Table 23. Temperature Sensor Range**

| <code>entoff</code>                                                                                                                         | <code>tsrange[1]</code> | <code>tsrange[0]</code> | Temp. range | Unit | Slope   | ADC8 LSB |
|---------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|-------------------------|-------------|------|---------|----------|
| 1                                                                                                                                           | 0                       | 0                       | –64 ... 64  | °C   | 8 mV/°C | 0.5 °C   |
| 1                                                                                                                                           | 0                       | 1                       | –64 ... 192 | °C   | 4 mV/°C | 1 °C     |
| 1                                                                                                                                           | 1                       | 0                       | 0 ... 128   | °C   | 8 mV/°C | 0.5 °C   |
| 1                                                                                                                                           | 1                       | 1                       | –40 ... 216 | °F   | 4 mV/°F | 1 °F     |
| 0*                                                                                                                                          | 1                       | 0                       | 0 ... 341   | °K   | 3 mV/°K | 1.333 °K |
| <b>*Note:</b> Absolute temperature mode, no temperature shift. This mode is only for test purposes. POR value of <code>EN_TOFF</code> is 1. |                         |                         |             |      |         |          |

Control to adjust the temperature sensor accuracy is available by adjusting the bandgap voltage. By enabling the `envbgcal` and using the `vbgtcal[3:0]` bits to trim the bandgap the temperature sensor accuracy may be fine tuned in the final application. The slope of the temperature sensor is very linear and monotonic but the exact accuracy or offset in temperature is difficult to control better than  $\pm 10$  °C. With the `vbgttrim` or bandgap trim though the initial temperature offset can be easily adjusted and be better than  $\pm 3$  °C.

The different ranges for the temperature sensor and ADC8 are demonstrated in Figure 27. The value of the ADC8 may be translated to a temperature reading by  $\text{ADC8Value} \times \text{ADC8 LSB} + \text{Lowest Temperature in Temp Range}$ . For instance for a `tsrange = 00`,  $\text{Temp} = \text{ADC8Value} \times 0.5 - 64$ .

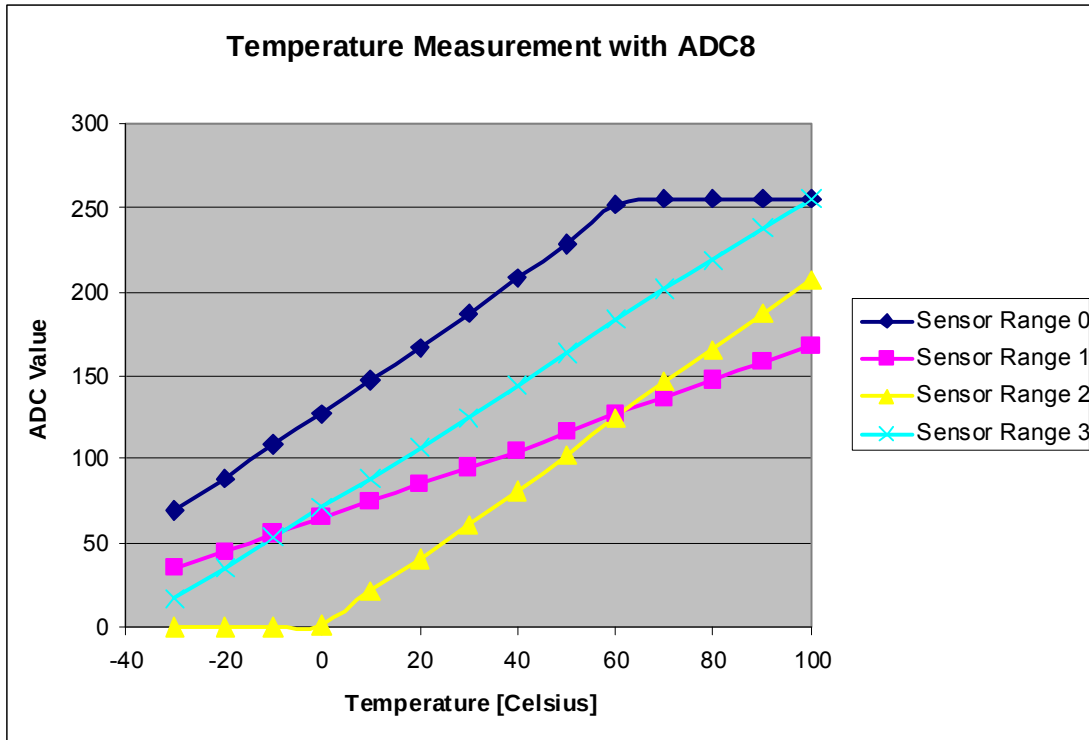


**Figure 27. Temperature Ranges using ADC8**

## 8.5. Low Battery Detector

A low battery detector (LBD) with digital read-out is integrated into the chip. A digital threshold may be programmed into the lbd[4:0] field in "Register 1Ah. Low Battery Detector Threshold". When the digitized battery voltage reaches this threshold an interrupt will be generated on the nIRQ pin to the microcontroller. The microcontroller will then need to verify the interrupt by reading "Register 03h. Interrupt/Status 1" and "Register 04h. Interrupt/Status 2," on page 87.

If the LBD is enabled while the chip is in SLEEP mode, it will automatically enable the RC oscillator which will periodically turn on the LBD circuit to measure the battery voltage. The battery voltage may also be read out through "Register 1Bh. Battery Voltage Level" at any time when the LBD is enabled. The Low Battery Detect function is enabled by setting enlbd=1 in "Register 07h. Operating Mode and Function Control 1".

| Ad | R/W | Function/Description           | D7 | D6 | D5 | D4      | D3      | D2      | D1      | D0      | POR Def. |
|----|-----|--------------------------------|----|----|----|---------|---------|---------|---------|---------|----------|
| 1A | R/W | Low Battery Detector Threshold |    |    |    | lbd[4]  | lbd[3]  | lbd[2]  | lbd[1]  | lbd[0]  | 14h      |
| 1B | R   | Battery Voltage Level          | 0  | 0  | 0  | vbat[4] | vbat[3] | vbat[2] | vbat[1] | vbat[0] | —        |

The LBD output is digitized by a 5-bit ADC. When the LBD function is enabled, enlbd = 1 in "Register 07h. Operating Mode and Function Control 1", the battery voltage may be read at anytime by reading "Register 1Bh. Battery Voltage Level". A Battery Voltage Threshold may be programmed to register 1Ah. When the battery voltage level drops below the battery voltage threshold an interrupt will be generated on nIRQ pin to the microcontroller if the LBD interrupt is enabled in "Register 06h. Interrupt Enable 2," on page 90. The microcontroller will then need to verify the interrupt by reading the interrupt status register, Addresses 03 and 04H. The LSB step size for the LBD ADC is 50 mV, with the ADC range demonstrated in the table below. If the LBD is enabled the LBD and ADC will automatically be enabled every 1 s for approximately 250  $\mu$ s to measure the voltage which minimizes the current consumption in Sensor mode. Before an interrupt is activated four consecutive readings are required.

$$\text{BatteryVoltage} = 1.7 + 50\text{mV} \times \text{ADCValue}$$

| ADC Value | VDD Voltage [V] |
|-----------|-----------------|
| 0         | < 1.7           |
| 1         | 1.7–1.75        |
| 2         | 1.75–1.8        |
| ...       | ...             |
| 29        | 3.1–3.15        |
| 30        | 3.15–3.2        |
| 31        | > 3.2           |

## 8.6. Wake-Up Timer

The chip contains an integrated wake-up timer which periodically wakes the chip from SLEEP mode. The wake-up timer runs from the internal 32.768 kHz RC Oscillator. The wake-up timer can be configured to run when in SLEEP mode. If  $enwt = 1$  in "Register 07h. Operating Mode and Function Control 1" when entering SLEEP mode, the wake-up timer will count for a time specified by the Wake-Up Timer Period in Registers 14h–16h. At the expiration of this period an interrupt will be generated on the nIRQ pin if this interrupt is enabled. The microcontroller will then need to verify the interrupt by reading the Interrupt Status Registers 03h–04h. The wake-up timer value may be read at any time by the  $wtv[15:0]$  read only registers 17h–18h.

The formula for calculating the Wake-Up Period is the following:

$$WUT = \frac{32 \times M \times 2^R}{32.768} ms$$

| WUT Register | Description        |
|--------------|--------------------|
| wtr[4:0]     | R Value in Formula |
| wtm[15:0]    | M Value in Formula |

Use of the D variable in the formula is only necessary if finer resolution is required than the R value gives.

| Add | R/W | Function/Description   | D7      | D6      | D5      | D4      | D3      | D2      | D1     | D0     | POR Def. |
|-----|-----|------------------------|---------|---------|---------|---------|---------|---------|--------|--------|----------|
| 14  | R/W | Wake-Up Timer Period 1 |         |         |         | wtr[4]  | wtr[3]  | wtr[2]  | wtr[1] | wtr[0] | 03h      |
| 15  | R/W | Wake-Up Timer Period 2 | wtm[15] | wtm[14] | wtm[13] | wtm[12] | wtm[11] | wtm[10] | wtm[9] | wtm[8] | 00h      |
| 16  | R/W | Wake-Up Timer Period 3 | wtm[7]  | wtm[6]  | wtm[5]  | wtm[4]  | wtm[3]  | wtm[2]  | wtm[1] | wtm[0] | 00h      |
| 17  | R   | Wake-Up Timer Value 1  | wtv[15] | wtv[14] | wtv[13] | wtv[12] | wtv[11] | wtv[10] | wtv[9] | wtv[8] | —        |
| 18  | R   | Wake-Up Timer Value 2  | wtv[7]  | wtv[6]  | wtv[5]  | wtv[4]  | wtv[3]  | wtv[2]  | wtv[1] | wtv[0] | —        |

There are two different methods for utilizing the wake-up timer (WUT) depending on if the WUT interrupt is enabled in "Register 06h. Interrupt Enable 2," on page 90. If the WUT interrupt is enabled then nIRQ pin will go low when the timer expires. The chip will also change state so that the 30 M XTAL is enabled so that the microcontroller clock output is available for the microcontroller to use process the interrupt. The other method of use is to not enable the WUT interrupt and use the WUT GPIO setting. In this mode of operation the chip will not change state until commanded by the microcontroller. The two different modes of operation of the WUT are demonstrated in Figure 28.

A 32 kHz XTAL may also be used for better timing accuracy. By setting the x32 ksel bit in 07h, GPIO0 is automatically reconfigured so that an external 32 kHz XTAL may be connected to this pin. In this mode, the GPIO0 is extremely sensitive to parasitic capacitance, so only the XTAL should be connected to this pin and the XTAL should be physically located as close to the pin as possible. Once the x32 ksel bit is set, all internal functions such as WUT, micro-controller clock, and LDC mode will use the 32 K XTAL and not the 32 kHz RC oscillator.

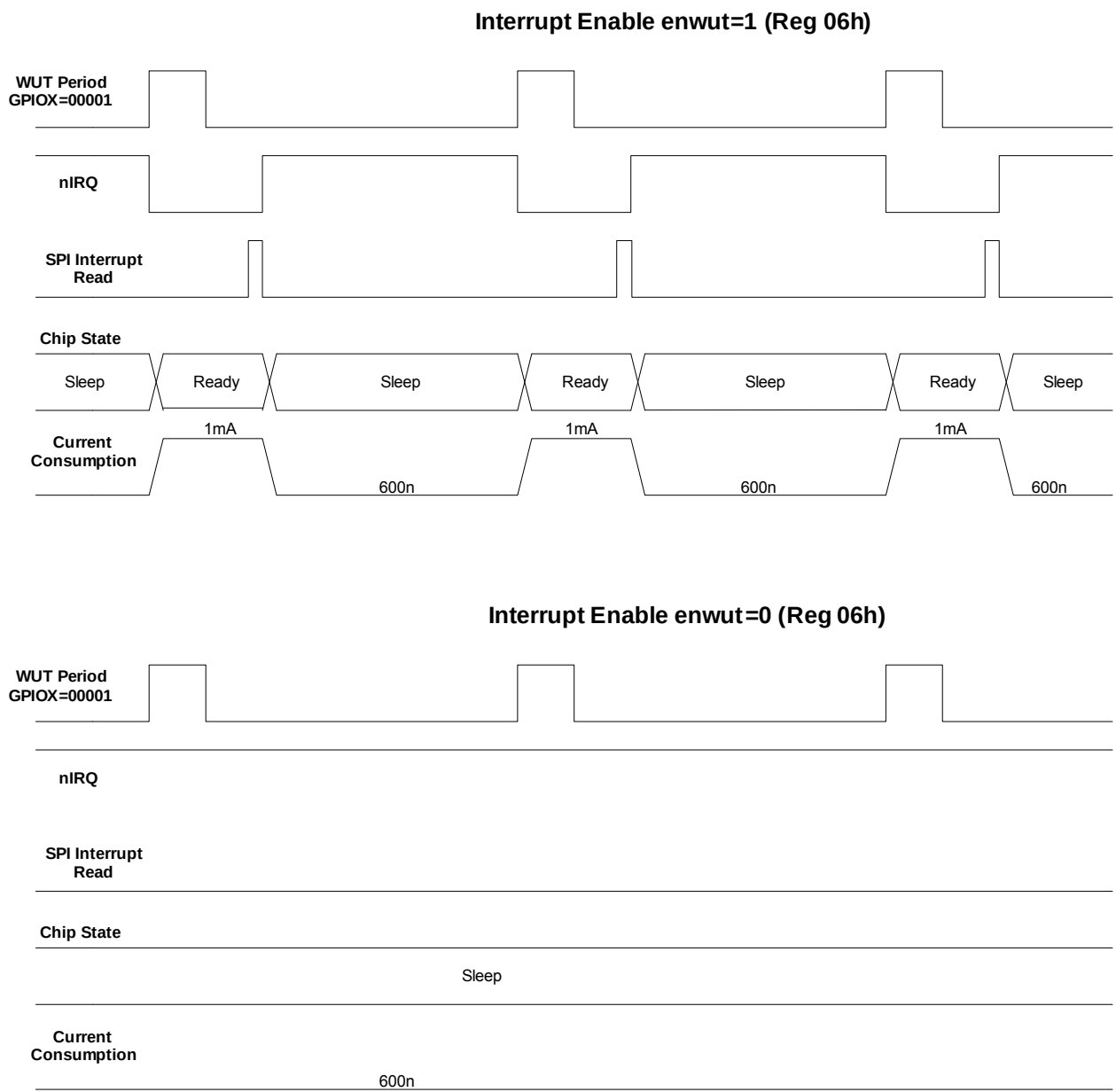


Figure 28. WUT Interrupt and WUT Operation

## 8.7. Low Duty Cycle Mode

The Low Duty Cycle Mode is available to automatically wake-up the receiver to check if a valid signal is available. The basic operation of the low duty cycle mode is demonstrated in the figure below. If a valid preamble or sync word is not detected the chip will return to sleep mode until the beginning of a new WUT period. If a valid preamble and sync are detected the receiver on period will be extended for the low duty cycle mode duration (TLDC) to receive all of the packet. The time of the TLDC is determined by the formula below:

$$TLDC = ldc [7 : 0] \times \frac{4 \times 2^R}{32 \cdot 768} ms$$

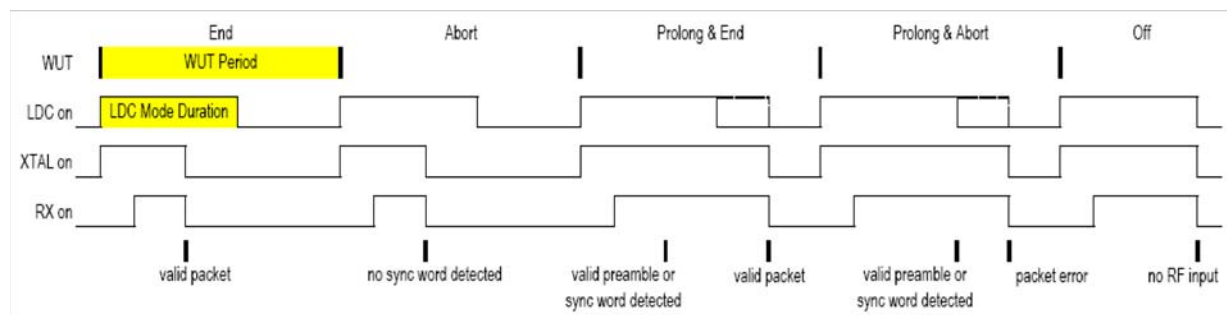


Figure 29. Low Duty Cycle Mode

## 8.8. GPIO Configuration

Three general purpose IOs (GPIOs) are available. Numerous functions such as specific interrupts, TRSW control, Microcontroller Output, etc. can be routed to the GPIO pins as shown in the tables below. When in Shutdown mode all the GPIO pads are pulled low.

**Note:** The ADC should not be selected as an input to the GPIO in Standby or Sleep Modes and will cause excess current consumption.

| Add | R/W | Function/Description   | D7          | D6          | D5         | D4         | D3       | D2       | D1       | D0       | POR Def. |
|-----|-----|------------------------|-------------|-------------|------------|------------|----------|----------|----------|----------|----------|
| 0B  | R/W | GPIO0 Configuration    | gpio0drv[1] | gpio0drv[0] | pup0       | gpio0[4]   | gpio0[3] | gpio0[2] | gpio0[1] | gpio0[0] | 00h      |
| 0C  | R/W | GPIO1 Configuration    | gpio1drv[1] | gpio1drv[0] | pup1       | gpio1[4]   | gpio1[3] | gpio1[2] | gpio1[1] | gpio1[0] | 00h      |
| 0D  | R/W | GPIO2 Configuration    | gpio2drv[1] | gpio2drv[0] | pup2       | gpio2[4]   | gpio2[3] | gpio2[2] | gpio2[1] | gpio2[0] | 00h      |
| 0E  | R/W | I/O Port Configuration |             | extitst[2]  | extitst[1] | extitst[0] | itsdo    | dio2     | dio1     | dio0     | 00h      |

The GPIO settings for GPIO1 and GPIO2 are the same as for GPIO0 with the exception of the 00000 default setting. The default settings for each GPIO are listed below:

| GPIO  | 00000—Default Setting |
|-------|-----------------------|
| GPIO0 | POR                   |
| GPIO1 | POR Inverted          |
| GPIO2 | Microcontroller Clock |

The chip is configured to provide the System Clock output to the microcontroller so that only one crystal is needed in the system, therefore reducing the BOM cost. For the TX Data Source, Direct Mode is used because long packets are desired with a unique packet handling format already implemented in the microcontroller. In this configuration the TX Data Clock is configured onto GPIO0, the TX Data is configured onto GPIO1, and the Microcontroller System Clock output is configured onto GPIO2.

For a complete list of the available GPIO's see "Register 0Ch. GPIO Configuration 1," on page 96, "Register 0Dh. GPIO Configuration 2," on page 97, and "Register 0Eh. I/O Port Configuration," on page 98.

## 8.9. Antenna-Diversity

To mitigate the problem of frequency-selective fading due to multi-path propagation, some transceiver systems use a scheme known as Antenna Diversity. In this scheme, two antennas are used. Each time the transceiver enters RX mode the receive signal strength from each antenna is evaluated. This evaluation process takes place during the preamble portion of the packet. The antenna with the strongest received signal is then used for the remainder of that RX packet. The same antenna will also be used for the next corresponding TX packet.

This chip fully supports Antenna Diversity with an integrated Antenna Diversity Control Algorithm. By setting GPIOx[4:0] = 10111 and 11000, the required signal needed to control an external SPDT RF switch (such as PIN diode or GaAs switch) is made available on the GPIOx pins. The operation of these switches is programmable to allow for different Antenna Diversity architectures and configurations. The antdiv[2:0] register is found in register 08h. The GPIO pin is capable of sourcing up to 5 mA of current, so it may be used directly to forward-bias a PIN diode if desired.

When the arrival of the packet is unknown by the receiver the antenna diversity algorithm (antdiv[2:0] = 100 or 101) will detect both packet arrival and selects the antenna with the strongest signal. The recommended preamble length to obtain good antenna selection is 8 bytes. A special antenna diversity algorithm (antdiv[2:0] = 110 or 111) is included that allows for shorter preamble for TDMA like systems where the arrival of the packet is synchronized to the receiver enable. The recommended preamble length to obtain good antenna selection for synchronized mode is 4 bytes.

| Add | R/W | Function/Description           | D7        | D6        | D5        | D4    | D3     | D2    | D1      | D0      | POR Def. |
|-----|-----|--------------------------------|-----------|-----------|-----------|-------|--------|-------|---------|---------|----------|
| 08  | R/W | Operating & Function Control 2 | antdiv[2] | antdiv[1] | antdiv[0] | rxmpk | autotx | enldm | ffclrrx | ffclrtx | 00h      |

**Table 24. Antenna Diversity Control**

| antdiv[2:0] | RX/TX State                                |           | Non RX/TX State |           |
|-------------|--------------------------------------------|-----------|-----------------|-----------|
|             | GPIO Ant1                                  | GPIO Ant2 | GPIO Ant1       | GPIO Ant2 |
| 000         | 0                                          | 1         | 0               | 0         |
| 001         | 1                                          | 0         | 0               | 0         |
| 010         | 0                                          | 1         | 1               | 1         |
| 011         | 1                                          | 0         | 1               | 1         |
| 100         | Antenna Diversity Algorithm                |           | 0               | 0         |
| 101         | Antenna Diversity Algorithm                |           | 1               | 1         |
| 110         | Antenna Diversity Algorithm in Beacon Mode |           | 0               | 0         |
| 111         | Antenna Diversity Algorithm in Beacon Mode |           | 1               | 1         |

## 8.10. RSSI and Clear Channel Assessment

The RSSI (Received Signal Strength Indicator) signal is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI value can be read from an 8-bit register with 0.5 dB resolution per bit. Figure 30 demonstrates the relationship between input power level and RSSI value. The RSSI may be read at anytime, but an incorrect error may rarely occur. The RSSI value may be incorrect if read during the update period. The update period is approximately 10 ns every 4 Tb. For 10 kbps, this would result in a 1 in 40,000 probability that the RSSI may be read incorrectly. This probability is extremely low, but to avoid this, one of the following options is recommended: majority polling, reading the RSSI value within 1 Tb of the RSSI interrupt, or using the RSSI threshold described in the next paragraph for Clear Channel Assessment.

| Add | R/W | Function/Description                       | D7        | D6        | D5        | D4        | D3        | D2        | D1        | D0        | POR Def. |
|-----|-----|--------------------------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|
| 26  | R   | Received Signal Strength Indicator         | rssi[7]   | rssi[6]   | rssi[5]   | rssi[4]   | rssi[3]   | rssi[2]   | rssi[1]   | rssi[0]   | —        |
| 27  | R/W | RSSI Threshold for Clear Channel Indicator | rssith[7] | rssith[6] | rssith[5] | rssith[4] | rssith[3] | rssith[2] | rssith[1] | rssith[0] | 00h      |

For Clear Channel Assessment a threshold is programmed into rssith[7:0] in "Register 27h. RSSI Threshold for Clear Channel Indicator". After the RSSI is evaluated in the preamble, a decision is made if the signal strength on this channel is above or below the threshold. If the signal strength is above the programmed threshold then a 1 will be shown in the RSSI status bit in "Register 02h. Device Status", "Register 04h. Interrupt/Status 2", or configurable GPIO (GPIO[3:0] = 1110).

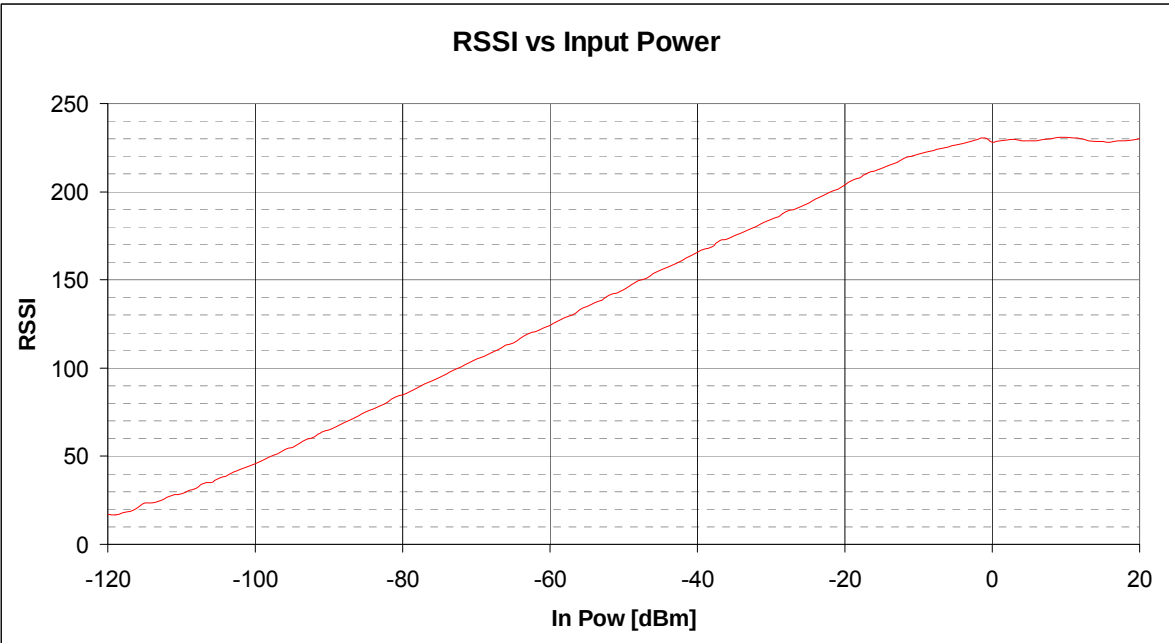


Figure 30. RSSI Value vs. Input Power

**Preliminary Rev. 0.4**

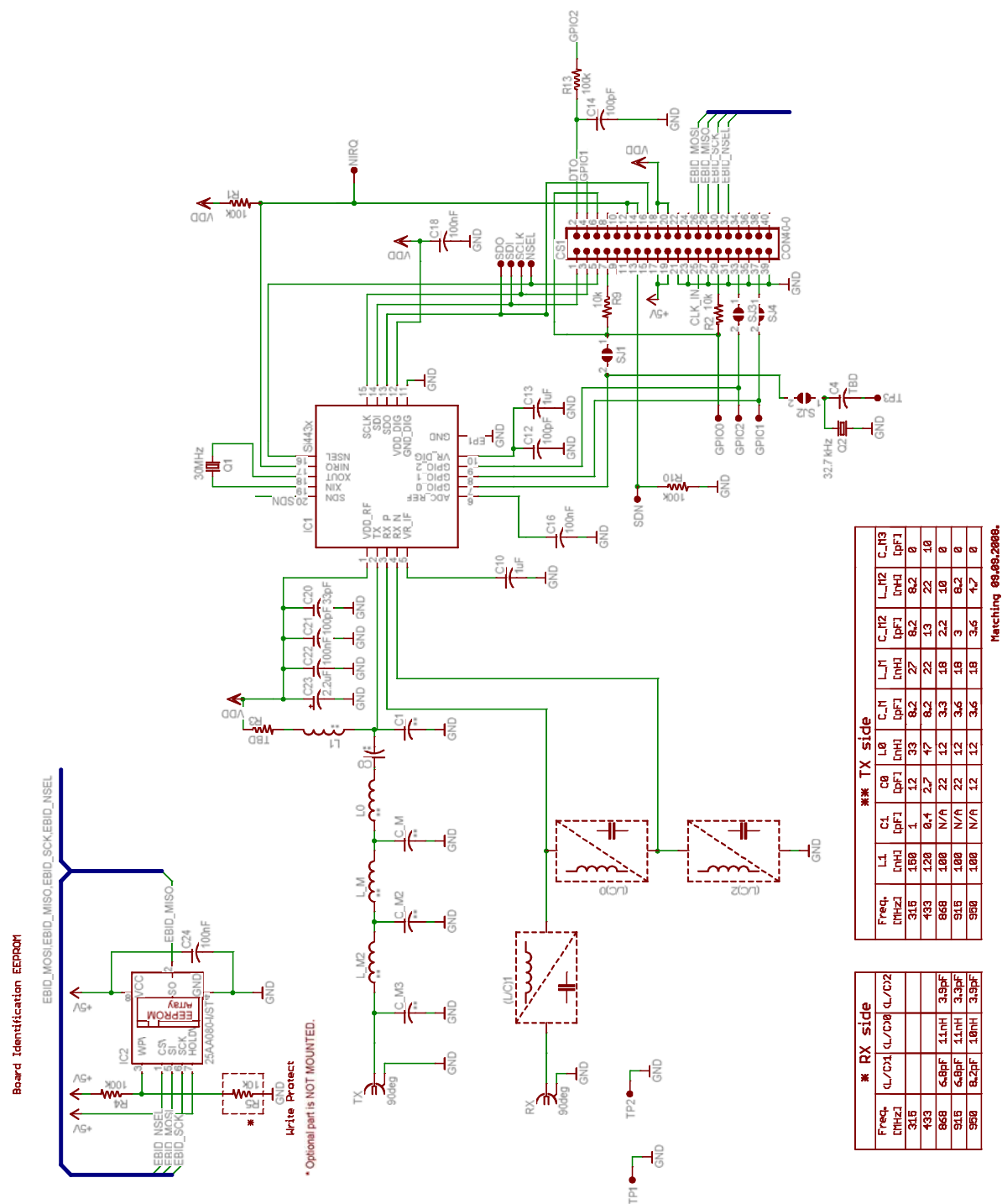


Table 25. Split RF I/Os Bill of Materials

| Part                                                                                                            | Value        | Device                   | Package           | Description                            |
|-----------------------------------------------------------------------------------------------------------------|--------------|--------------------------|-------------------|----------------------------------------|
| (L/C)0                                                                                                          | **           | Inductor/Capacitor **    | 0603              | Coilcraft 0603CS / Murata GRM18 series |
| (L/C)1                                                                                                          | **           | Inductor/Capacitor **    | 0603              | Coilcraft 0603CS / Murata GRM18 series |
| (L/C)2                                                                                                          | **           | Inductor/Capacitor **    | 0603              | Coilcraft 0603CS / Murata GRM18 series |
| C0                                                                                                              | **           | Capacitor                | 0603              | Murata GRM18 series                    |
| C1                                                                                                              | **           | Capacitor                | 0603              | Murata GRM18 series                    |
| C4                                                                                                              | TBD          | Capacitor                | 0603              | Murata GRM18 series                    |
| C10                                                                                                             | 1uF          | Capacitor                | 0603              | Murata GRM18 series                    |
| C12                                                                                                             | 100pF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C13                                                                                                             | 1uF          | Capacitor                | 0603              | Murata GRM18 series                    |
| C14                                                                                                             | 100pF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C16                                                                                                             | 100nF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C18                                                                                                             | 100nF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C20                                                                                                             | 33pF         | Capacitor                | 0603              | Murata GRM18 series                    |
| C21                                                                                                             | 100pF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C22                                                                                                             | 100nF        | Capacitor                | 0603              | Murata GRM18 series                    |
| C23                                                                                                             | 2.2uF        | POLARIZED CAPACITOR      | 0804              | POLARIZED CAPACITOR                    |
| C24                                                                                                             | 100nF        | Capacitor                | 0603              | Murata GRM18 series                    |
| CS1                                                                                                             | CON40-0      | CON40-0                  | PANDUIT-057-040-0 | 40-PIN male connector, 90° deg         |
| C_M                                                                                                             | **           | Capacitor                | 0603              | Murata GRM18 series                    |
| C_M2                                                                                                            | **           | Capacitor                | 0603              | Murata GRM18 series                    |
| C_M3                                                                                                            | **           | Capacitor                | 0603              | Murata GRM18 series                    |
| IC1                                                                                                             | Si4431       | Si4431                   | QFN-20            | Silicon Lab's RF transceiver IC        |
| IC2                                                                                                             | 25AA080-I/ST | 25AA080ST                | TSSOP8            | Serial EEPROM                          |
| L0                                                                                                              | **           | Inductor                 | 0603              | Coilcraft 0603CS                       |
| L1                                                                                                              | **           | Inductor                 | 0603              | Coilcraft 0603CS                       |
| L_M                                                                                                             | **           | Inductor                 | 0603              | Coilcraft 0603CS                       |
| L_M2                                                                                                            | **           | Inductor                 | 0603              | Coilcraft 0603CS                       |
| Q1                                                                                                              | 30MHz        | CRYSTAL-4PINSX-2520-NEW1 | N/A               | SIWARD 2520                            |
| Q2                                                                                                              | 32.7 kHz     | CRYSTAL32SL              | N/A               | SMQ32SL                                |
| R1                                                                                                              | 100k         | Resistor                 | 0603              |                                        |
| R2                                                                                                              | 10k          | Resistor                 | 0603              |                                        |
| R3                                                                                                              | TBD          | Resistor                 | 0603              |                                        |
| R4                                                                                                              | 100k         | Resistor                 | 0603              |                                        |
| R5                                                                                                              | 10k          | Resistor                 | 0603              |                                        |
| R9                                                                                                              | 10k          | Resistor                 | 0603              |                                        |
| R10                                                                                                             | 100k         | Resistor                 | 0603              |                                        |
| R13                                                                                                             | 100k         | Resistor                 | 0603              |                                        |
| RX                                                                                                              | 90deg        | BU-SMA-RADIAL            | BU-SMA-V          | 90°degree bent, female SMA connector   |
| TX                                                                                                              | 90deg        | BU-SMA-RADIAL            | BU-SMA-V          | 90°degree bent, female SMA connector   |
| <b>**Note:</b> For exact values please find the schematic's table with the appropriate matching network values. |              |                          |                   |                                        |

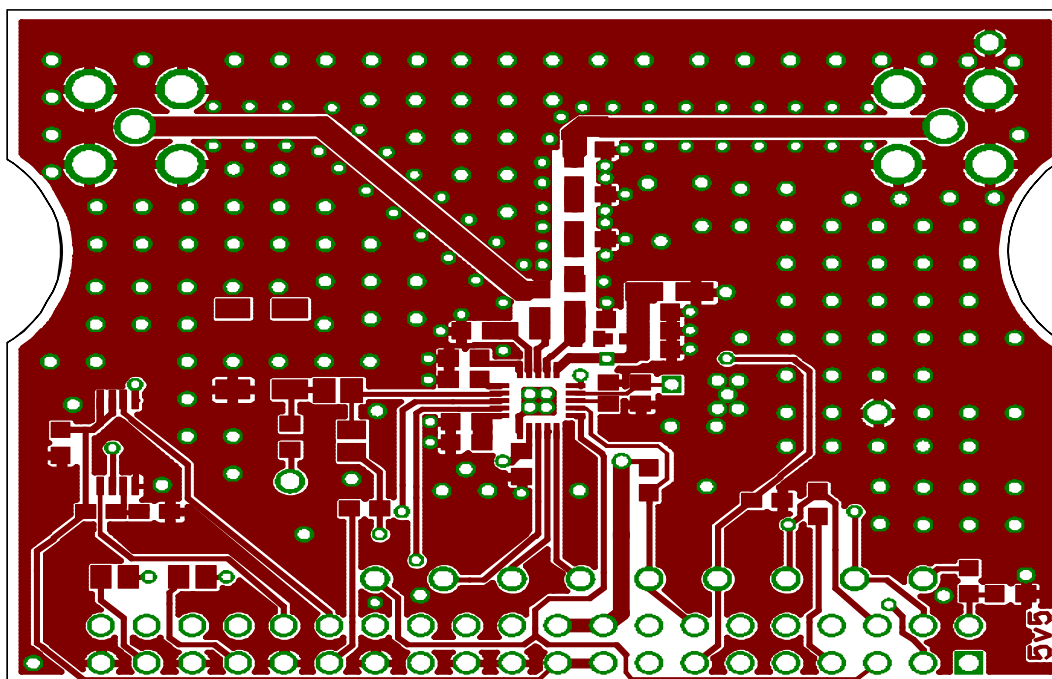


Figure 32. Split RF I/Os with Separated TX and RX Connectors—Top

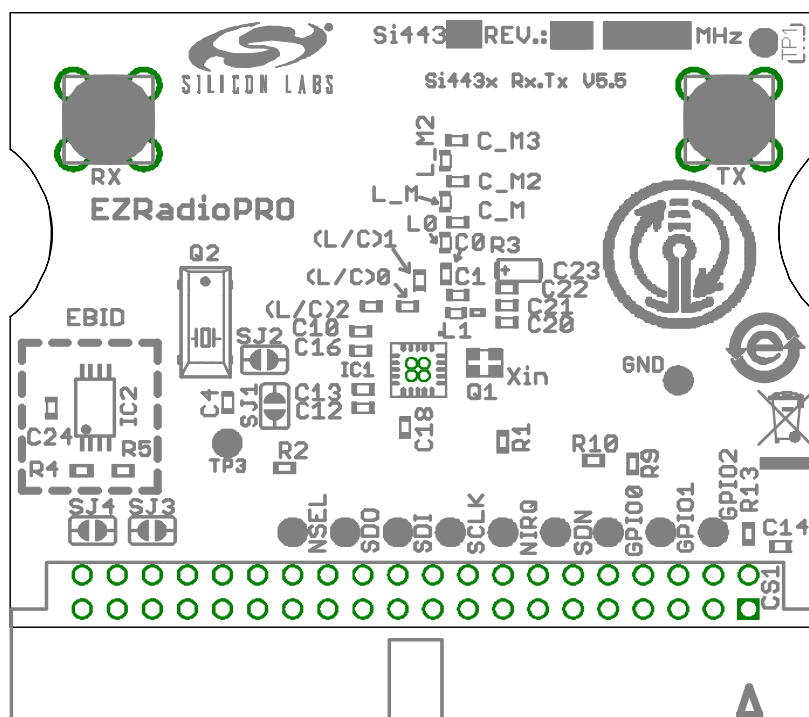


Figure 33. Split RF I/Os with Separated TX and RX Connectors—Top Silkscreen

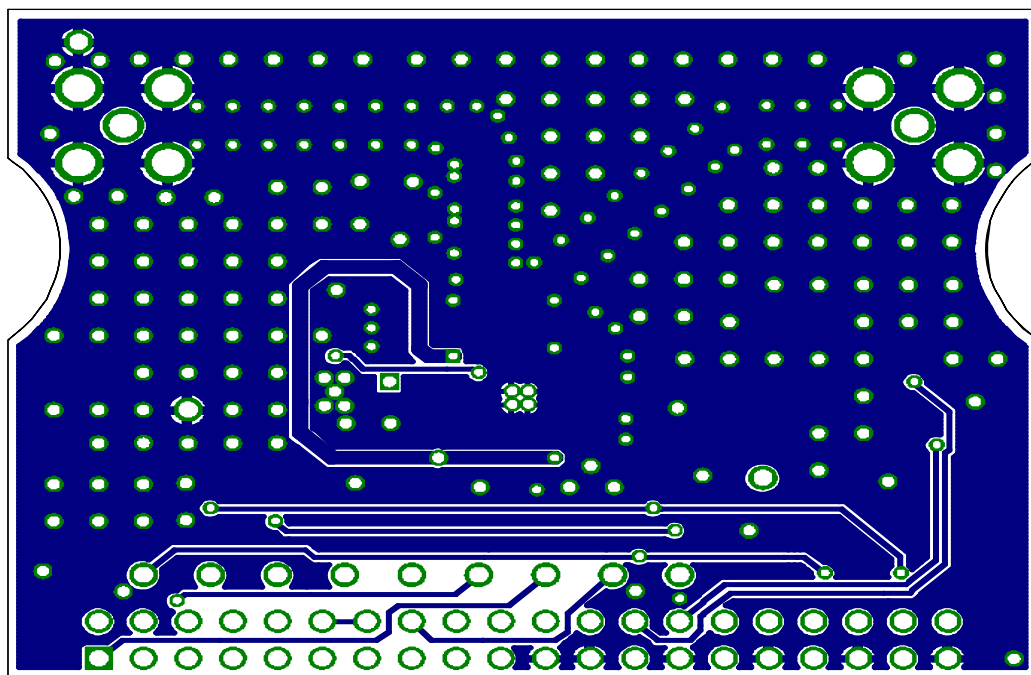
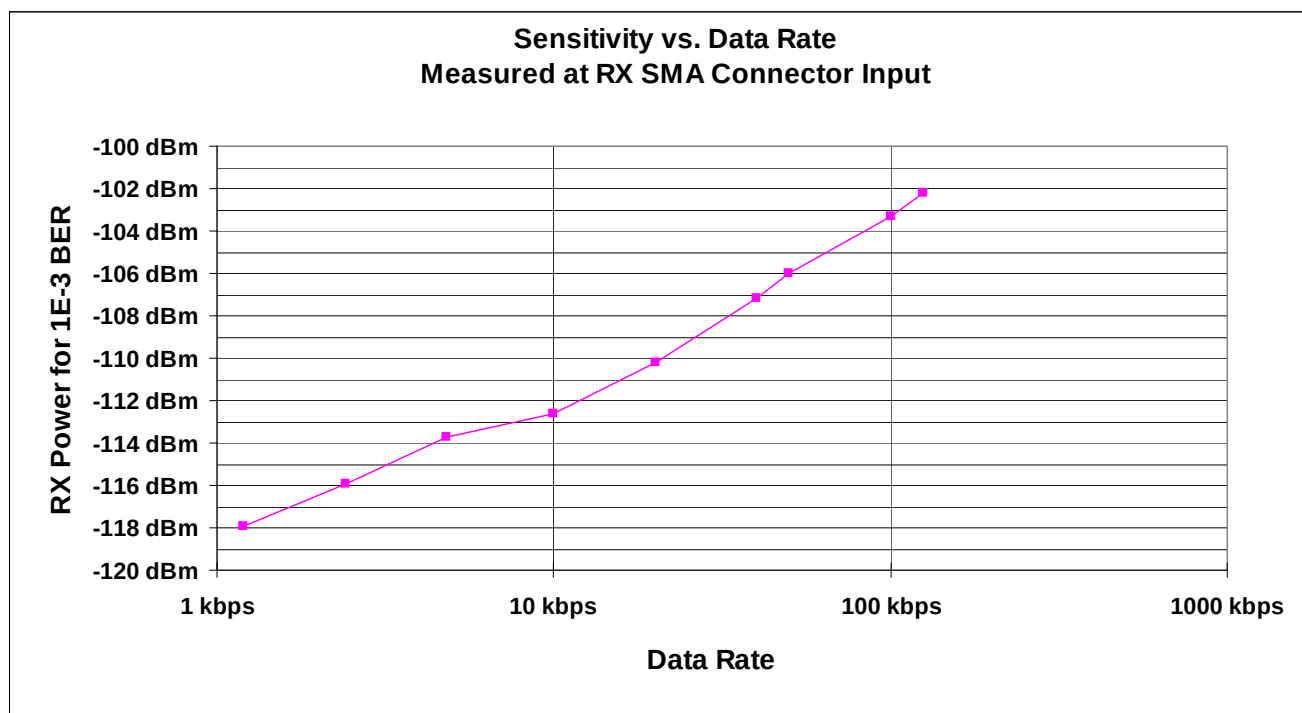


**Figure 34. Split RF I/Os with Separated TX and RX Connectors—Bottom**

**Note:** The reference design shown above is the that of the standard testcard that may be ordered directly from Silicon Labs. Within this reference design is a EEPROM called the EBID (Evaluation Board IDentification). The EBID is used by other Silicon Labs development tools and is not required on customer designs.

## 10. Measurement Results



**Note:** Sensitivity is BER measured, GFSK modulation, BT = 0.5, H = 1.

**Figure 35. Sensitivity vs. Data Rate**

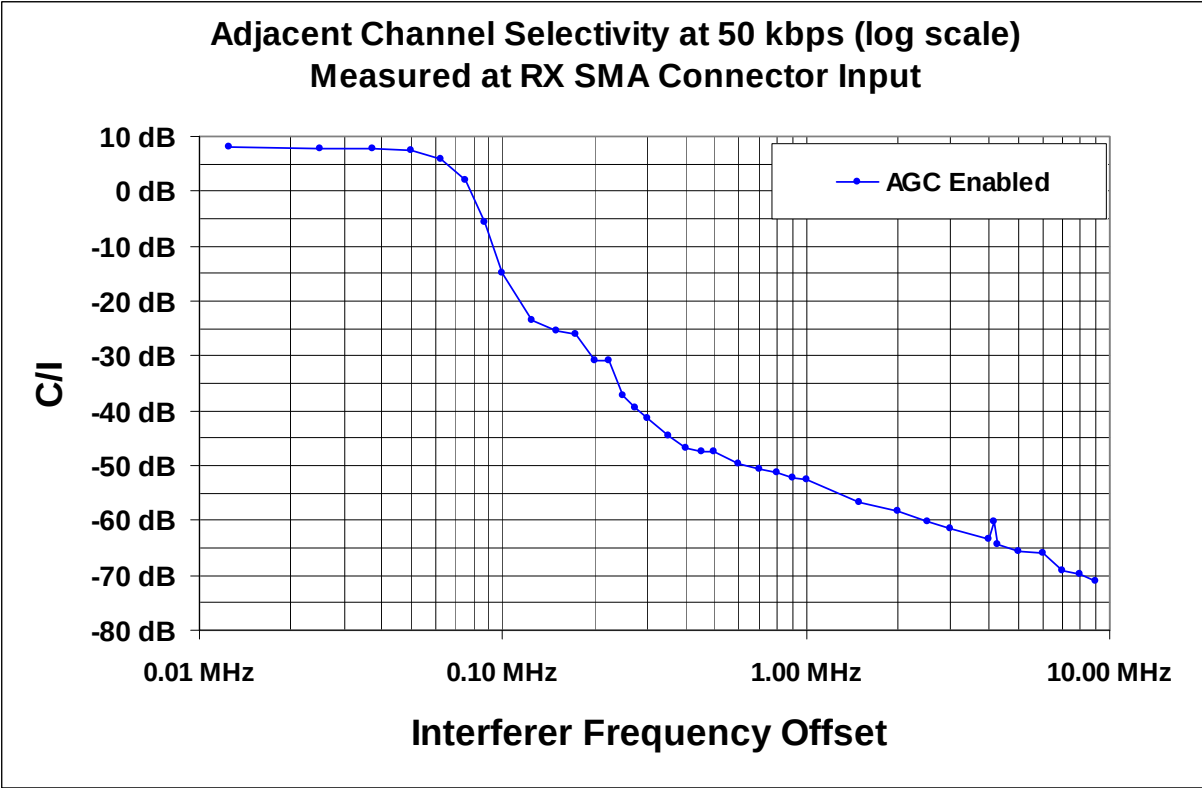
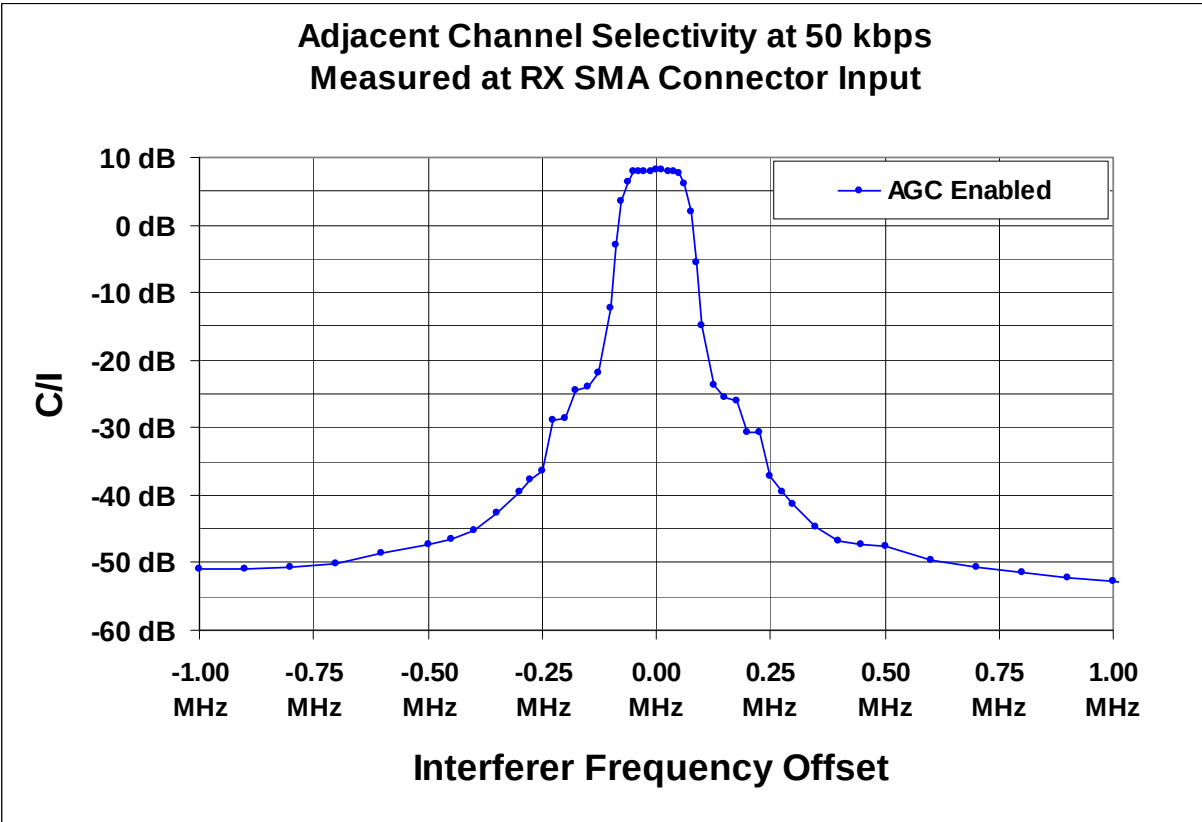


Figure 36. Receiver Selectivity

Date: 04-22-08 Time: 02:28 PM

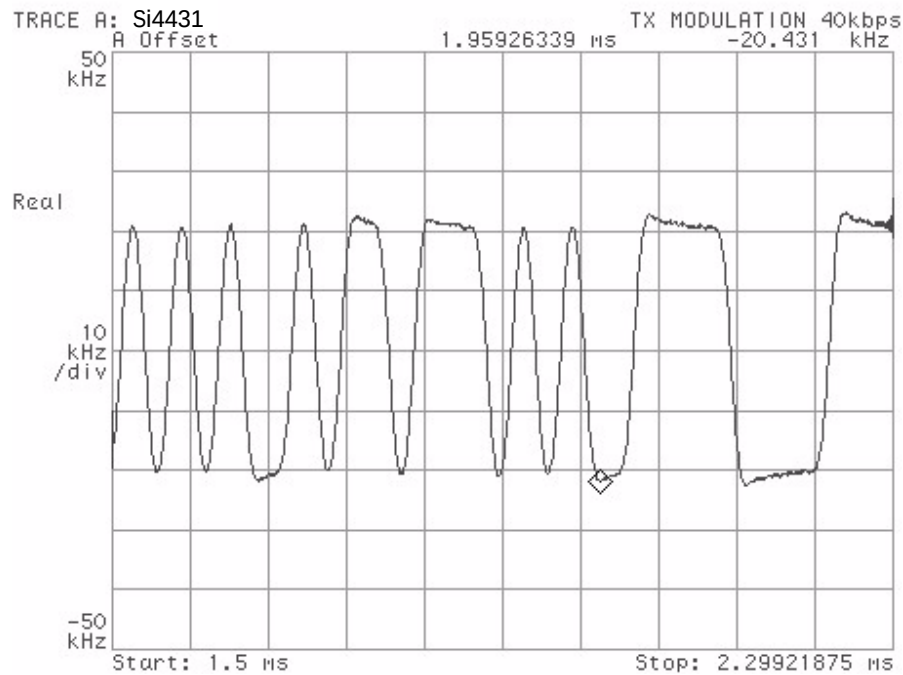


Figure 37. TX Modulation (40 kbps, 20 kHz Deviation)

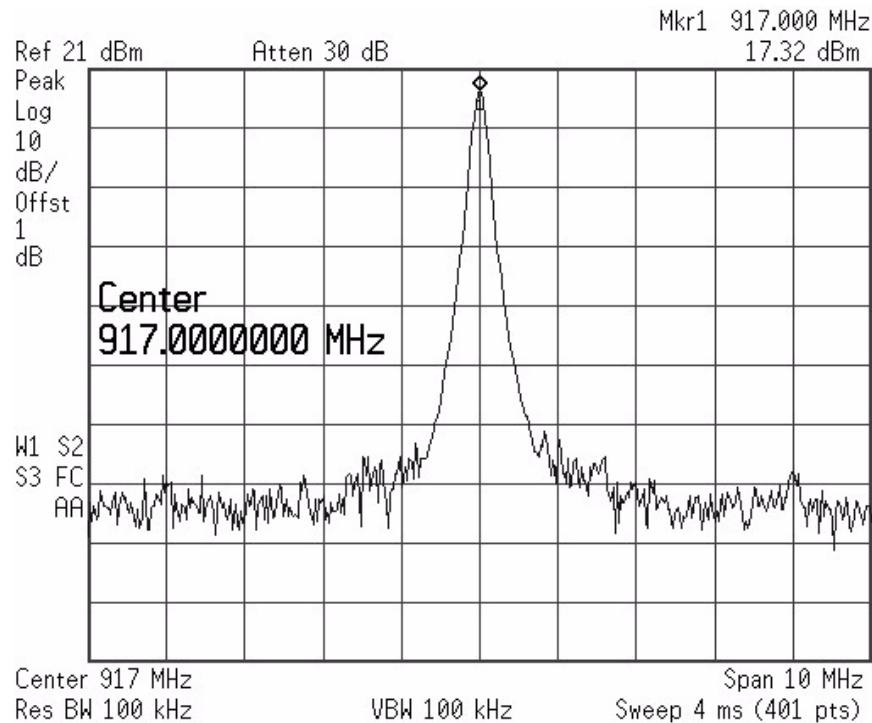


Figure 38. TX Unmodulated Spectrum (917 MHz)

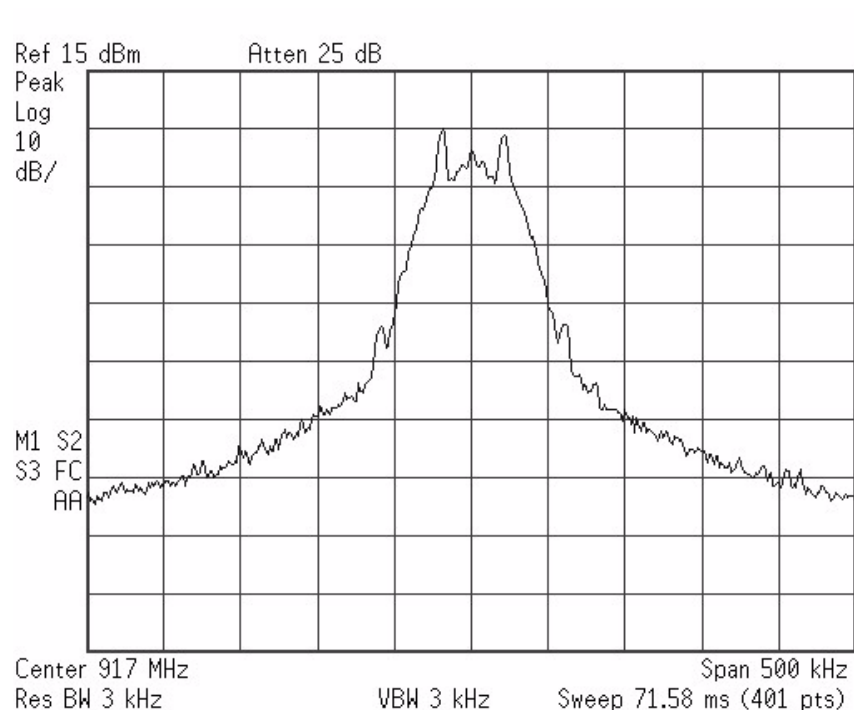


**Figure 39. TX Modulated Spectrum (917 MHz, 40 kbps, 20 kHz Deviation, GFSK)**

**Date: 04-23-08    Time: 04:03 PM**

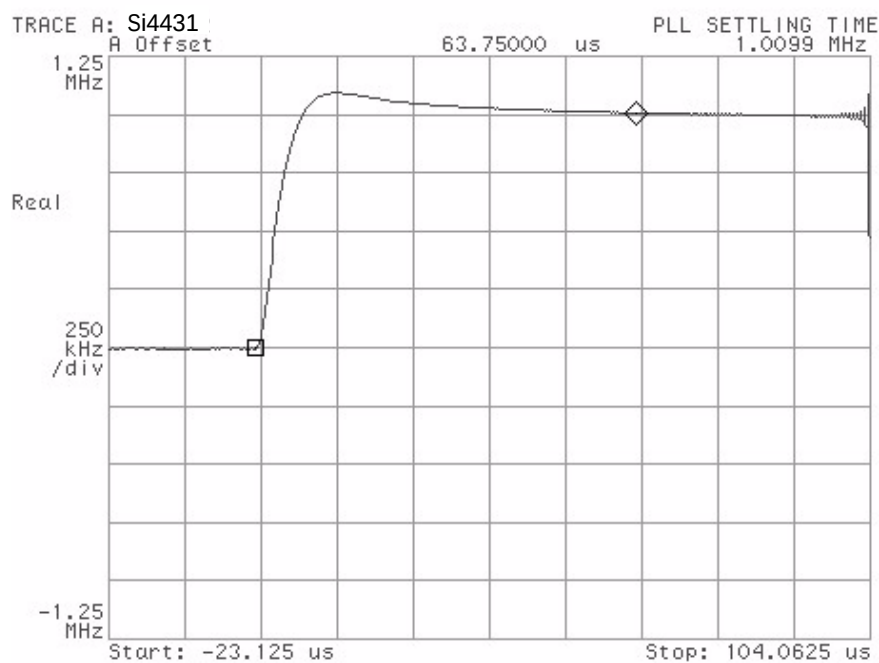


**Figure 40. Synthesizer Settling Time for 1 MHz Jump Settled within 10 kHz**

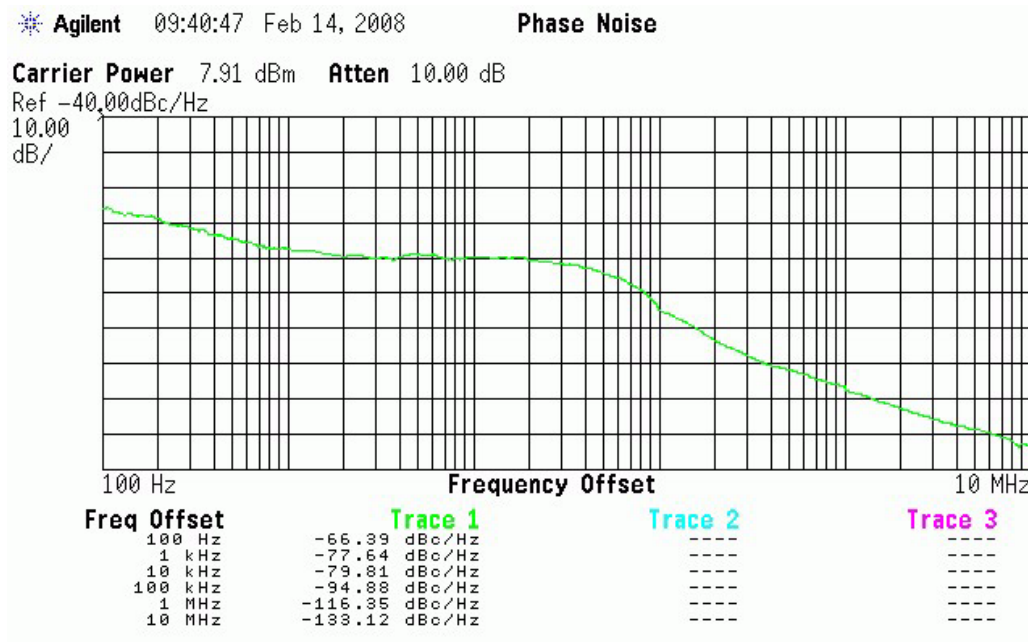


Figure 41. Synthesizer Phase Noise (VCOCURR = 11)

## 11. Application Notes

### 11.1. Crystal Selection

The recommended crystal parameters are given in Table 26.

**Table 26. Recommended Crystal Parameters**

| Frequency | ESR         | C <sub>L</sub> | C <sub>0</sub> | Frequency Accuracy |
|-----------|-------------|----------------|----------------|--------------------|
| 30 MHz    | 60 $\Omega$ | 12 pF          | 5 pF           | $\pm 20$ ppm       |

The internal XTAL oscillator will work over a range for the parameters of ESR, CL, C0, and ppm accuracy. Extreme values may affect the XTAL start-up and sensitivity of the link. For questions regarding the use of a crystal parameters greatly deviating from the recommend values listed above, please contact customer support.

The crystal used for engineering evaluation and the reference design is the SIWARD –SX2520– 30.0 MHz – 12.0R. Ordering number XTL581200JIG.

### 11.2. Layout Practice

The following are some general best practice guidelines for PCB layout using the EZRadioPro devices:

- Bypass capacitors should be placed as close as possible to the pin.
- TX/RX matching/layout should mimic reference as much as possible. Failing to do so may cause loss in performance.
- A solid ground plane is required on the backside of the board under TX/RX matching components
- Crystal should be placed as close as possible to the XIN/XOUT pins and should not have VDD traces running underneath or near it.
- The paddle on the backside of the QFN package needs solid grounding and good soldered connection
- Use GND stitch vias liberally throughout the board, especially underneath the paddle.

## 11.3. Matching Network Design

### 11.3.1. RX LNA Matching

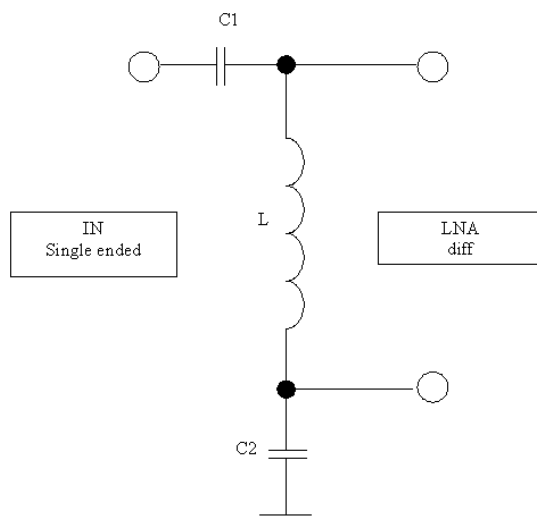


Figure 42. RX LNA Matching

Table 27. RX Matching for Different Bands

| Freq Band | C1      | L       | C2     |
|-----------|---------|---------|--------|
| 915 MHz   | 6.8 pF  | 11.0 nH | 3.3 pF |
| 868 MHz   | 6.8 pF  | 11.0 nH | 3.9 pF |
| 433 MHz   | 10.0 pF | 33.0 nH | 4.7 pF |
| 315 MHz   | 15.0 pF | 47.0 nH | 5.6 pF |

### 11.3.2. TX PA Matching and Filtering

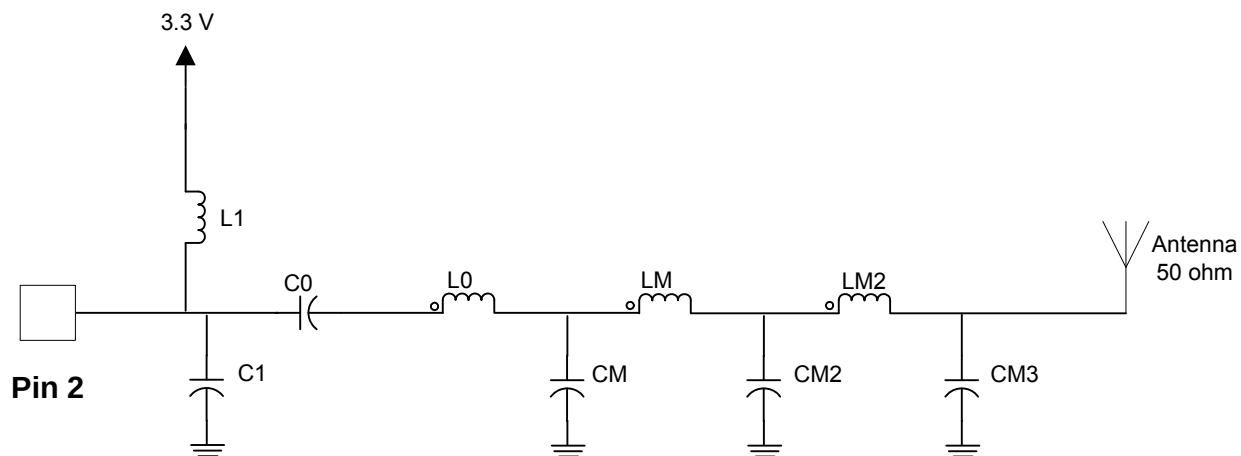


Figure 43. TX Matching and Filtering for Different Bands

# Si4431

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| Freq Band | L1       | C1     | C0      | L0      | CM     | LM      | CM2     | LM2     | CM3     |
|-----------|----------|--------|---------|---------|--------|---------|---------|---------|---------|
| 915 MHz   | 100.0 nH | N/A    | 22.0 pF | 12.0 nH | 3.6 pF | 18.0 nH | 3.0 pF  | 8.2 nH  | N/A     |
| 868 MHz   | 100.0 nH | N/A    | 22.0 pF | 12.0 nH | 3.3 pF | 18.0 nH | 2.2 pF  | 10.0 nH | N/A     |
| 433 MHz   | 120.0 nH | 0.4 pF | 2.7 pF  | 47.0 nH | 8.2 pF | 22.0 nH | 13.0 pF | 22.0 nH | 10.0 pF |
| 315 MHz   | 150.0 nH | 1.0 pF | 12.0 pF | 33.0 nH | 8.2 pF | 27.0 nH | 8.2 pF  | 8.2 nH  | N/A     |

## 12. Reference Material

### 12.1. Complete Register Table and Descriptions

Table 28. Register Descriptions

| Add | R/W | Function/Desc                              | Data              |             |             |             |             |             |             |             | POR Default |
|-----|-----|--------------------------------------------|-------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|     |     |                                            | D7                | D6          | D5          | D4          | D3          | D2          | D1          | D0          |             |
| 00  | R   | Device Type                                | 0                 | 0           | 0           | dt[4]       | dt[3]       | dt[2]       | dt[1]       | dt[0]       | 00111       |
| 01  | R   | Device Version                             | 0                 | 0           | 0           | vc[4]       | vc[3]       | vc[2]       | vc[1]       | vc[0]       | 04h         |
| 02  | R   | Device Status                              | ffovfl            | ffunfl      | rxffem      | headerr     | reserved    | reserved    | cps[1]      | cps[0]      | —           |
| 03  | R   | Interrupt Status 1                         | ifferr            | itxffaull   | itxffaem    | irxffaull   | ixext       | ipksent     | ipkvalid    | icrcerror   | —           |
| 04  | R   | Interrupt Status 2                         | iswdet            | ipreaval    | ipreainval  | irssi       | iwut        | ilbd        | ichiprdy    | ipor        | —           |
| 05  | R/W | Interrupt Enable 1                         | enfferr           | entxffaull  | entxffaem   | enrxffaull  | enext       | enpkpsent   | enpkvalid   | enrcerror   | 00h         |
| 06  | R/W | Interrupt Enable 2                         | enswdet           | enpreaval   | enpreainval | enrssi      | enwut       | enlbd       | enchiprdy   | enpor       | 03h         |
| 07  | R/W | Operating & Function Control 1             | swres             | enlbd       | enwt        | x32ksel     | txon        | rxon        | pllon       | xton        | 01h         |
| 08  | R/W | Operating & Function Control 2             | antdiv[2]         | antdiv[1]   | antdiv[0]   | rxmpk       | autotx      | enldm       | ffclrx      | ffclrtx     | 00h         |
| 09  | R/W | Crystal Oscillator Load Capacitance        | xtalshft          | xlcl[6]     | xlcl[5]     | xlcl[4]     | xlcl[3]     | xlcl[2]     | xlcl[1]     | xlcl[0]     | 7Fh         |
| 0A  | R/W | Microcontroller Output Clock               | Reserved          | Reserved    | Reserved    | clkt[0]     | enlfc       | mclk[2]     | mclk[1]     | mclk[0]     | 06h         |
| 0B  | R/W | GPIO0 Configuration                        | gpio0drv[1]       | gpio0drv[0] | pup0        | gpio0[4]    | gpio0[3]    | gpio0[2]    | gpio0[1]    | gpio0[0]    | 00h         |
| 0C  | R/W | GPIO1 Configuration                        | gpio1drv[1]       | gpio1drv[0] | pup1        | gpio1[4]    | gpio1[3]    | gpio1[2]    | gpio1[1]    | gpio1[0]    | 00h         |
| 0D  | R/W | GPIO2 Configuration                        | gpio2drv[1]       | gpio2drv[0] | pup2        | gpio2[4]    | gpio2[3]    | gpio2[2]    | gpio2[1]    | gpio2[0]    | 00h         |
| 0E  | R/W | I/O Port Configuration                     | Reserved          | Reserved    | extitst[2]  | extitst[1]  | extitst[0]  | itsdo       | dio2        | dio0        | 00h         |
| 0F  | R/W | ADC Configuration                          | adcstart/adc-done | adcsl[2]    | adcsl[1]    | adcsl[0]    | adcref[1]   | adcref[0]   | adcgain[1]  | adcgain[0]  | 00h         |
| 10  | R/W | ADC Sensor Amplifier Offset                | Reserved          | Reserved    | Reserved    | Reserved    | adcoffs[3]  | adcoffs[2]  | adcoffs[1]  | adcoffs[0]  | 00h         |
| 11  | R   | ADC Value                                  | adc[7]            | adc[6]      | adc[5]      | adc[4]      | adc[3]      | adc[2]      | adc[1]      | adc[0]      | —           |
| 12  | R/W | Temperature Sensor Control                 | tsrange[1]        | tsrange[0]  | entsoffs    | entstrim    | tstrim[3]   | tstrim[2]   | tstrim[1]   | tstrim[0]   | 20h         |
| 13  | R/W | Temperature Value Offset                   | tvofts[7]         | tvofts[6]   | tvofts[5]   | tvofts[4]   | tvofts[3]   | tvofts[2]   | tvofts[1]   | tvofts[0]   | 00h         |
| 14  | R/W | Wake-Up Timer Period 1                     | Reserved          | Reserved    | Reserved    | wtr[4]      | wtr[3]      | wtr[2]      | wtr[1]      | wtr[0]      | 03h         |
| 15  | R/W | Wake-Up Timer Period 2                     | wtm[15]           | wtm[14]     | wtm[13]     | wtm[12]     | wtm[11]     | wtm[10]     | wtm[9]      | wtm[8]      | 00h         |
| 16  | R/W | Wake-Up Timer Period 3                     | wtm[7]            | wtm[6]      | wtm[5]      | wtm[4]      | wtm[3]      | wtm[2]      | wtm[1]      | wtm[0]      | 01h         |
| 17  | R   | Wake-Up Timer Value 1                      | wtv[15]           | wtv[14]     | wtv[13]     | wtv[12]     | wtv[11]     | wtv[10]     | wtv[9]      | wtv[8]      | —           |
| 18  | R   | Wake-Up Timer Value 2                      | wtv[7]            | wtv[6]      | wtv[5]      | wtv[4]      | wtv[3]      | wtv[2]      | wtv[1]      | wtv[0]      | —           |
| 19  | R/W | Low-Duty Cycle Mode Duration               | ldc[7]            | ldc[6]      | ldc[5]      | ldc[4]      | ldc[3]      | ldc[2]      | ldc[1]      | ldc[0]      | 00h         |
| 1A  | R/W | Low Battery Detector Threshold             | Reserved          | Reserved    | Reserved    | lbd[4]      | lbd[3]      | lbd[2]      | lbd[1]      | lbd[0]      | 14h         |
| 1B  | R   | Battery Voltage Level                      | 0                 | 0           | 0           | vbat[4]     | vbat[3]     | vbat[2]     | vbat[1]     | vbat[0]     | —           |
| 1C  | R/W | IF Filter Bandwidth                        | dwn3_bypass       | ndec[2]     | ndec[1]     | ndec[0]     | filset[3]   | filset[2]   | filset[1]   | filset[0]   | 01h         |
| 1D  | R/W | AFC Loop Gearshift Override                | afcbd             | enafc       | afcgearh[2] | afcgearh[1] | afcgearl[0] | afcgearl[2] | afcgearl[1] | afcgearl[0] | 40h         |
| 1E  | R/W | AFC Timing Control                         | Reserved          | Reserved    | shwait[2]   | shwait[1]   | shwait[0]   | anwait[2]   | anwait[1]   | anwait[0]   | 0Ah         |
| 1F  | R/W | Clock Recovery Gearshift Override          | Reserved          | rxready     | crfast[2]   | crfast[1]   | crfast[0]   | crslow[2]   | crslow[1]   | crslow[0]   | 03h         |
| 20  | R/W | Clock Recovery Oversampling Ratio          | rxosr[7]          | rxosr[6]    | rxosr[5]    | rxosr[4]    | rxosr[3]    | rxosr[2]    | rxosr[1]    | rxosr[0]    | 64h         |
| 21  | R/W | Clock Recovery Offset 2                    | rxosr[10]         | rxosr[9]    | rxosr[8]    | stallctrl   | ncoff[19]   | ncoff[18]   | ncoff[17]   | ncoff[16]   | 01h         |
| 22  | R/W | Clock Recovery Offset 1                    | ncoff[15]         | ncoff[14]   | ncoff[13]   | ncoff[12]   | ncoff[11]   | ncoff[10]   | ncoff[9]    | ncoff[8]    | 47h         |
| 23  | R/W | Clock Recovery Offset 0                    | ncoff[7]          | ncoff[6]    | ncoff[5]    | ncoff[4]    | ncoff[3]    | ncoff[2]    | ncoff[1]    | ncoff[0]    | AEh         |
| 24  | R/W | Clock Recovery Timing Loop Gain 1          | Reserved          | Reserved    | Reserved    | Reserved    | Reserved    | crgain[10]  | crgain[9]   | crgain[8]   | 02h         |
| 25  | R/W | Clock Recovery Timing Loop Gain 0          | crgain[7]         | crgain[6]   | crgain[5]   | crgain[4]   | crgain[3]   | crgain[2]   | crgain[1]   | crgain[0]   | 8Fh         |
| 26  | R   | Received Signal Strength Indicator         | rss[7]            | rss[6]      | rss[5]      | rss[4]      | rss[3]      | rss[2]      | rss[1]      | rss[0]      | —           |
| 27  | R/W | RSSI Threshold for Clear Channel Indicator | rssith[7]         | rssith[6]   | rssith[5]   | rssith[4]   | rssith[3]   | rssith[2]   | rssith[1]   | rssith[0]   | 1Eh         |
| 28  | R   | Antenna Diversity Register 1               | adrssi[7]         | adrssia[6]  | adrssia[5]  | adrssia[4]  | adrssia[3]  | adrssia[2]  | adrssia[1]  | adrssia[0]  | —           |
| 29  | R   | Antenna Diversity Register 2               | adrssib[7]        | adrssib[6]  | adrssib[5]  | adrssib[4]  | adrssib[3]  | adrssib[2]  | adrssib[1]  | adrssib[0]  | —           |
| 2A  | R/W | AFC Limiter                                | Afclim[7]         | Afclim[6]   | Afclim[5]   | Afclim[4]   | Afclim[3]   | Afclim[2]   | Afclim[1]   | Afclim[0]   | 00h         |
| 2B  | R   | AFC Correction Read                        | afc_corr[9]       | afc_corr[8] | afc_corr[7] | afc_corr[6] | afc_corr[5] | afc_corr[4] | afc_corr[3] | afc_corr[2] | 00h         |
| 2C  | R/W | OOK Counter Value 1                        | afc_corr[9]       | afc_corr[9] | ookfrzen    | peakdeten   | madeten     | ookcnt[10]  | ookcnt[9]   | ookcnt[8]   | 18h         |
| 2D  | R/W | OOK Counter Value 2                        | ookcnt[7]         | ookcnt[6]   | ookcnt[5]   | ookcnt[4]   | ookcnt[3]   | ookcnt[2]   | ookcnt[1]   | ookcnt[0]   | BCh         |
| 2E  | R/W | Slicer Peak Hold                           | Reserved          | attack[2]   | attack[1]   | attack[0]   | decay[3]    | decay[2]    | decay[1]    | decay[0]    | 26h         |
| 2F  |     | Reserved                                   |                   |             |             |             |             |             |             |             |             |
| 30  | R/W | Data Access Control                        | enpacrx           | lsbfrst     | crdonly     | Reserved    | enpactx     | enrcrc      | crc[1]      | crc[0]      | 1Dh         |
| 31  | R   | EzMAC status                               | 0                 | rxcrcl      | pksrcr      | pkrx        | pkvalid     | crerror     | pktx        | pkscnt      | —           |
| 32  | R/W | Header Control 1                           | bcen[3:0]         |             |             |             | hdch[3:0]   |             |             |             | 0Ch         |
| 33  | R/W | Header Control 2                           | Reserved          | hdlen[2]    | hdlen[1]    | hdlen[0]    | fixpkl      | syncncl[1]  | syncncl[0]  | prealen[8]  | 22h         |
| 34  | R/W | Preamble Length                            | prealen[7]        | prealen[6]  | prealen[5]  | prealen[4]  | prealen[3]  | prealen[2]  | prealen[1]  | prealen[0]  | 08h         |
| 35  | R/W | Preamble Detection Control                 | preath[4]         | preath[3]   | preath[2]   | preath[1]   | preath[0]   | rsi_off[2]  | rsi_off[1]  | rsi_off[0]  | 2Ah         |
| 36  | R/W | Sync Word 3                                | sync[31]          | sync[30]    | sync[29]    | sync[28]    | sync[27]    | sync[26]    | sync[25]    | sync[24]    | 2Dh         |
| 37  | R/W | Sync Word 2                                | sync[23]          | sync[22]    | sync[21]    | sync[20]    | sync[19]    | sync[18]    | sync[17]    | sync[16]    | D4h         |
| 38  | R/W | Sync Word 1                                | sync[15]          | sync[14]    | sync[13]    | sync[12]    | sync[11]    | sync[10]    | sync[9]     | sync[8]     | 00h         |
| 39  | R/W | Sync Word 0                                | sync[7]           | sync[6]     | sync[5]     | sync[4]     | sync[3]     | sync[2]     | sync[1]     | sync[0]     | 00h         |
| 3A  | R/W | Transmit Header 3                          | txhd[31]          | txhd[30]    | txhd[29]    | txhd[28]    | txhd[27]    | txhd[26]    | txhd[25]    | txhd[24]    | 00h         |
| 3B  | R/W | Transmit Header 2                          | txhd[23]          | txhd[22]    | txhd[21]    | txhd[20]    | txhd[19]    | txhd[18]    | txhd[17]    | txhd[16]    | 00h         |
| 3C  | R/W | Transmit Header 1                          | txhd[15]          | txhd[14]    | txhd[13]    | txhd[12]    | txhd[11]    | txhd[10]    | txhd[9]     | txhd[8]     | 00h         |

Table 28. Register Descriptions (Continued)

| Add   | R/W | Function/Desc                             | Data            |               |               |               |               |                |              |                | POR Default |
|-------|-----|-------------------------------------------|-----------------|---------------|---------------|---------------|---------------|----------------|--------------|----------------|-------------|
|       |     |                                           | D7              | D6            | D5            | D4            | D3            | D2             | D1           | D0             |             |
| 3D    | R/W | Transmit Header 0                         | txhd[7]         | txhd[6]       | txhd[5]       | txhd[4]       | txhd[3]       | txhd[2]        | txhd[1]      | txhd[0]        | 00h         |
| 3E    | R/W | Transmit Packet Length                    | pklen[7]        | pklen[6]      | pklen[5]      | pklen[4]      | pklen[3]      | pklen[2]       | pklen[1]     | pklen[0]       | 00h         |
| 3F    | R/W | Check Header 3                            | chhd[31]        | chhd[30]      | chhd[29]      | chhd[28]      | chhd[27]      | chhd[26]       | chhd[25]     | chhd[24]       | 00h         |
| 40    | R/W | Check Header 2                            | chhd[23]        | chhd[22]      | chhd[21]      | chhd[20]      | chhd[19]      | chhd[18]       | chhd[17]     | chhd[16]       | 00h         |
| 41    | R/W | Check Header 1                            | chhd[15]        | chhd[14]      | chhd[13]      | chhd[12]      | chhd[11]      | chhd[10]       | chhd[9]      | chhd[8]        | 00h         |
| 42    | R/W | Check Header 0                            | chhd[7]         | chhd[6]       | chhd[5]       | chhd[4]       | chhd[3]       | chhd[2]        | chhd[1]      | chhd[0]        | 00h         |
| 43    | R/W | Header Enable 3                           | hden[31]        | hden[30]      | hden[29]      | hden[28]      | hden[27]      | hden[26]       | hden[25]     | hden[24]       | FFh         |
| 44    | R/W | Header Enable 2                           | hden[23]        | hden[22]      | hden[21]      | hden[20]      | hden[19]      | hden[18]       | hden[17]     | hden[16]       | FFh         |
| 45    | R/W | Header Enable 1                           | hden[15]        | hden[14]      | hden[13]      | hden[12]      | hden[11]      | hden[10]       | hden[9]      | hden[8]        | FFh         |
| 46    | R/W | Header Enable 0                           | hden[7]         | hden[6]       | hden[5]       | hden[4]       | hden[3]       | hden[2]        | hden[1]      | hden[0]        | FFh         |
| 47    | R   | Received Header 3                         | rxhd[31]        | rxhd[30]      | rxhd[29]      | rxhd[28]      | rxhd[27]      | rxhd[26]       | rxhd[25]     | rxhd[24]       | —           |
| 48    | R   | Received Header 2                         | rxhd[23]        | rxhd[22]      | rxhd[21]      | rxhd[20]      | rxhd[19]      | rxhd[18]       | rxhd[17]     | rxhd[16]       | —           |
| 49    | R   | Received Header 1                         | rxhd[15]        | rxhd[14]      | rxhd[13]      | rxhd[12]      | rxhd[11]      | rxhd[10]       | rxhd[9]      | rxhd[8]        | —           |
| 4A    | R   | Received Header 0                         | rxhd[7]         | rxhd[6]       | rxhd[5]       | rxhd[4]       | rxhd[3]       | rxhd[2]        | rxhd[1]      | rxhd[0]        | —           |
| 4B    | R   | Received Packet Length                    | rxplen[7]       | rxplen[6]     | rxplen[5]     | rxplen[4]     | rxplen[3]     | rxplen[2]      | rxplen[1]    | rxplen[0]      | —           |
| 4C-4E |     |                                           | Reserved        |               |               |               |               |                |              |                |             |
| 4F    | R/W | ADC8 Control                              | Reserved        | Reserved      | adc8[5]       | adc8[4]       | adc8[3]       | adc8[2]        | adc8[1]      | adc8[0]        | 00h         |
| 50    | R/W | Analog Test Bus                           | Reserved        | Reserved      | Reserved      | atb[4]        | atb[3]        | atb[2]         | atb[1]       | atb[0]         | 00h         |
| 51    | R/W | Digital Test Bus                          | Reserved        | ensctest      | dtb[5]        | dtb[4]        | dtb[3]        | dtb[2]         | dtb[1]       | dtb[0]         | 00h         |
| 52    | R/W | TX Ramp Control                           | Reserved        | txmod[2]      | txmod[1]      | txmod[0]      | ldoramp[1]    | ldoramp[0]     | txramp[1]    | txramp[0]      | 2Fh         |
| 53    | R/W | PLL Tune Time                             | pllt[4]         | pllt[3]       | pllt[2]       | pllt[1]       | pllt[0]       | pllt0[2]       | pllt0[1]     | pllt0[0]       | 52h         |
| 54    | R/W | Invalid Preamble Threshold and PA Misc    | Reserved        | Reserved      | inv_pre_th[3] | inv_pre_th[2] | inv_pre_th[1] | inv_pre_th[0]  | ldo_pa_boost | pa_vbias_boost | 14h         |
| 55    | R/W | Calibration Control                       | Reserved        | xtalstarthalf | adccaldone    | enrcfcal      | rcal          | vcocaldp       | vcocal       | skipvco        | 44h         |
| 56    | R/W | Modem Test                                | bcrfbyp         | slifbyp       | dttype        | oscdeten      | OOKth         | refclkssel     | refclkinv    | distogg        | 00h         |
| 57    | R/W | Chargepump Test                           | pfdrst          | fbdiv_rst     | cpforcedn     | cdonly        | cdccur[2]     | cdccur[1]      | cdccur[0]    | cdccur[0]      | 00h         |
| 58    | R/W | Chargepump Current Trimming/Override      | cpcurr[1]       | cpcurr[0]     | cpccorrov     | cpccorr[4]    | cpccorr[3]    | cpccorr[2]     | cpccorr[1]   | cpccorr[0]     | 80h         |
| 59    | R/W | Divider Current Trimming                  | txcorboosten    | fbdivhc       | d3trim[1]     | d3trim[0]     | d2trim[1]     | d2trim[0]      | d1p5trim[1]  | d1p5trim[0]    | 40h         |
| 5A    | R/W | VCO Current Trimming                      | txcurboosten    | vcocorrov     | vcocorr[3]    | vcocorr[2]    | vcocorr[1]    | vcocorr[0]     | vcocur[1]    | vcocur[0]      | 03h         |
| 5B    | R/W | VCO Calibration / Override                | vcocalov/vcdone | vcocal[6]     | vcocal[5]     | vcocal[4]     | vcocal[3]     | vcocal[2]      | vcocal[1]    | vcocal[0]      | 00h         |
| 5C    | R/W | Synthesizer Test                          | dsmdt           | vcotype       | enolop        | dsmod         | dsorder[1]    | dsorder[0]     | dsrstmod     | dsrst          | 0Eh         |
| 5D    | R/W | Block Enable Override 1                   | enmix           | enlna         | enp3a         | enpa          | enbf5         | endv32         | enbf12       | enmx2          | 00h         |
| 5E    | R/W | Block Enable Override 2                   | ends            | enldet        | enmx3         | enbf4         | enbf3         | enbf11         | enbf2        | pllreset       | 40h         |
| 5F    | R/W | Block Enable Override 3                   | enfrdv          | endv31        | endv2         | endv1p5       | dvbshunt      | envco          | enncp        | enbg           | 00h         |
| 60    | R/W | Channel Filter Coefficient Address        | Reserved        | Reserved      | Reserved      | Reserved      | chfiladd[3]   | chfiladd[2]    | chfiladd[1]  | chfiladd[0]    | 00h         |
| 61    | R/W | Channel Filter Coefficient Value          | Reserved        | Reserved      | chfilval[5]   | chfilval[4]   | chfilval[3]   | chfilval[2]    | chfilval[1]  | chfilval[0]    | 00h         |
| 62    | R/W | Crystal Oscillator / Control Test         | pwtst[2]        | pwtst[1]      | pwtst[0]      | clkhyst       | enbias2x      | enamp2x        | bufovr       | enbuf          | 24h         |
| 63    | R/W | RC Oscillator Coarse Calibration/Override | rccov           | rcf[6]        | rcf[5]        | rcf[4]        | rcf[3]        | rcf[2]         | rcf[1]       | rcf[0]         | 00h         |
| 64    | R/W | RC Oscillator Fine Calibration/Override   | rcfov           | rcf[6]        | rcf[5]        | rcf[4]        | rcf[3]        | rcf[2]         | rcf[1]       | rcf[0]         | 00h         |
| 65    | R/W | LDO Control Override                      | enspor          | enbias        | envcoldo      | enifldo       | enrldo        | enplldo        | endigldo     | endigpwn       | 81h         |
| 66    | R/W | LDO Level Setting                         | enovr           | enxtal        | ents          | enrc32        | Reserved      | diglvi[2]      | diglvi[1]    | diglvi[0]      | 02h         |
| 67    | R/W | Delta Sigma ADC Tuning 1                  | adcrst          | enrefdac      | enadc         | adctuneovr    | adctune[3]    | adctune[2]     | adctune[1]   | adctune[0]     | 1Dh         |
| 68    | R/W | Delta Sigma ADC Tuning 2                  | Reserved        | Reserved      | Reserved      | envcm         | adcoloop      | adcref[2]      | adcref[1]    | adcref[0]      | 03h         |
| 69    | R/W | AGC Override 1                            | Reserved        | Reserved      | agcen         | lnagain       | pga3          | pga2           | pga1         | pga0           | 20h         |
| 6A    | R/W | AGC Override 2                            | agcovpm         | agcslow       | lnacomp[3]    | lnacomp[2]    | lnacomp[1]    | lnacomp[0]     | pgath[1]     | pgath[0]       | 1Dh         |
| 6B    | R/W | GFSK FIR Filter Coefficient Address       | Reserved        | Reserved      | Reserved      | Reserved      | Reserved      | firadd[2]      | firadd[1]    | firadd[0]      | 00h         |
| 6C    | R/W | GFSK FIR Filter Coefficient Value         | Reserved        | Reserved      | firval[5]     | firval[4]     | firval[3]     | firval[2]      | firval[1]    | firval[0]      | 01h         |
| 6D    | R/W | TX Power                                  | Reserved        | Reserved      | Reserved      | Reserved      | lna_sw        | txpow[2]       | txpow[1]     | txpow[0]       | 08h         |
| 6E    | R/W | TX Data Rate 1                            | txdr[15]        | txdr[14]      | txdr[13]      | txdr[12]      | txdr[11]      | txdr[10]       | txdr[9]      | txdr[8]        | 0Ah         |
| 6F    | R/W | TX Data Rate 0                            | txdr[7]         | txdr[6]       | txdr[5]       | txdr[4]       | txdr[3]       | txdr[2]        | txdr[1]      | txdr[0]        | 3Dh         |
| 70    | R/W | Modulation Mode Control 1                 | Reserved        | Reserved      | txdtrtscale   | enphpwn       | manppol       | enmaninv       | enmanch      | enwhite        | 0Ch         |
| 71    | R/W | Modulation Mode Control 2                 | trclk[1]        | trclk[0]      | dtmod[1]      | dtmod[0]      | enin          | fd[8]          | modtyp[1]    | modtyp[0]      | 00h         |
| 72    | R/W | Frequency Deviation                       | fd[7]           | fd[6]         | fd[5]         | fd[4]         | fd[3]         | fd[2]          | fd[1]        | fd[0]          | 20h         |
| 73    | R/W | Frequency Offset 1                        | fo[7]           | fo[6]         | fo[5]         | fo[4]         | fo[3]         | fo[2]          | fo[1]        | fo[0]          | 00h         |
| 74    | R/W | Frequency Offset 2                        | Reserved        | Reserved      | Reserved      | Reserved      | Reserved      | Reserved       | fo[9]        | fo[8]          | 00h         |
| 75    | R/W | Frequency Band Select                     | Reserved        | sbsel         | hbsel         | fb[4]         | fb[3]         | fb[2]          | fb[1]        | fb[0]          | 75h         |
| 76    | R/W | Nominal Carrier Frequency 1               | fc[15]          | fc[14]        | fc[13]        | fc[12]        | fc[11]        | fc[10]         | fc[9]        | fc[8]          | BBh         |
| 77    | R/W | Nominal Carrier Frequency 0               | fc[7]           | fc[6]         | fc[5]         | fc[4]         | fc[3]         | fc[2]          | fc[1]        | fc[0]          | 80h         |
| 78    | R/W | Miscellaneous Settings                    | Reserved        | Reserved      | Reserved      | Reserved      | Alt_PA_Seq    | rcosc[2]       | rcosc[1]     | rcosc[0]       | 09h         |
| 79    | R/W | Frequency Hopping Channel Select          | fhch[7]         | fhch[6]       | fhch[5]       | fhch[4]       | fhch[3]       | fhch[2]        | fhch[1]      | fhch[0]        | 00h         |
| 7A    | R/W | Frequency Hopping Step Size               | fhs[7]          | fhs[6]        | fhs[5]        | fhs[4]        | fhs[3]        | fhs[2]         | fhs[1]       | fhs[0]         | 00h         |
| 7B    | R/W | Turn Around and 15.4 Length Compliance    | 15.4 Length     | Reserved      | Reserved      | Reserved      | Reserved      | turn_around_en | Phase[1]     | Phase[0]       | 09h         |
| 7C    | R/W | TX FIFO Control 1                         | Reserved        | Reserved      | txafthr[5]    | txafthr[4]    | txafthr[3]    | txafthr[2]     | txafthr[1]   | txafthr[0]     | 37h         |
| 7D    | R/W | TX FIFO Control 2                         | Reserved        | Reserved      | txaethr[5]    | txaethr[4]    | txaethr[3]    | txaethr[2]     | txaethr[1]   | txaethr[0]     | 04h         |
| 7E    | R/W | TX FIFO Control                           | Reserved        | Reserved      | rxafthr[5]    | rxafthr[4]    | rxafthr[3]    | rxafthr[2]     | rxafthr[1]   | rxafthr[0]     | 37h         |
| 7F    | R/W | FIFO Access                               | fifod[7]        | fifod[6]      | fifod[5]      | fifod[4]      | fifod[3]      | fifod[2]       | fifod[1]     | fifod[0]       | —           |

**Register 00h. Device Type Code (DT)**

| Bit         | D7       | D6 | D5 | D4      | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|---------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | dt[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R       |    |    |    |    |

Reset value = 00001000

| Bit | Name     | Function                                       |
|-----|----------|------------------------------------------------|
| 7:5 | Reserved | <b>Reserved.</b>                               |
| 4:0 | dt[4:0]  | <b>Device Type Code.</b><br>EZRadioPRO: 01000. |

**Register 01h. Version Code (VC)**

| Bit         | D7       | D6 | D5 | D4      | D3 | D2 | D1 | D0 |
|-------------|----------|----|----|---------|----|----|----|----|
| <b>Name</b> | Reserved |    |    | vc[4:0] |    |    |    |    |
| <b>Type</b> | R        |    |    | R       |    |    |    |    |

Reset value = xxxxxxxx

| Bit | Name     | Function                                                                          |
|-----|----------|-----------------------------------------------------------------------------------|
| 7:5 | Reserved | <b>Reserved.</b>                                                                  |
| 4:0 | vc[4:0]  | <b>Version Code.</b><br>Code indicating the version of the chip.<br>Rev A0: 00100 |

## Register 02h. Device Status

| Bit  | D7     | D6     | D5     | D4      | D3       | D2       | D1       | D0 |
|------|--------|--------|--------|---------|----------|----------|----------|----|
| Name | ffovfl | ffunfl | rxffem | headerr | Reserved | Reserved | cps[1:0] |    |
| Type | R      | R      | R      | R       | R        | R        | R        |    |

Reset value = xxxxxxxx

| Bit | Name     | Function                                                                                  |
|-----|----------|-------------------------------------------------------------------------------------------|
| 7   | ffovfl   | <b>RX/TX FIFO Overflow Status.</b>                                                        |
| 6   | ffunfl   | <b>RX/TX FIFO Underflow Status.</b>                                                       |
| 5   | rxffem   | <b>RX FIFO Empty Status.</b>                                                              |
| 4   | headerr  | <b>Header Error Status.</b><br>Indicates if the received packet has a header check error. |
| 3:2 | Reserved | <b>Reserved.</b>                                                                          |
| 1:0 | cps[1:0] | <b>Chip Power State.</b><br>00: Idle State<br>01: RX State<br>10: TX State                |

**Register 03h. Interrupt/Status 1**

| Bit  | D7     | D6        | D5       | D4        | D3   | D2      | D1       | D0        |
|------|--------|-----------|----------|-----------|------|---------|----------|-----------|
| Name | ifferr | itxffaull | ixtffaem | irxffaull | iext | ipksent | ipkvalid | icrcerror |
| Type | R      | R         | R        | R         | R    | R       | R        | R         |

Reset value = xxxxxxxx

| Bit | Name      | Function                                                                                                                                                                                                   |
|-----|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ifferr    | <b>FIFO Underflow/Overflow Error.</b><br>When set to 1 the TX or RX FIFO has overflowed or underflowed.                                                                                                    |
| 6   | itxffaull | <b>TX FIFO Almost Full.</b><br>When set to 1 the TX FIFO has met its almost full threshold and needs to be transmitted.                                                                                    |
| 5   | ixtffaem  | <b>TX FIFO Almost Empty.</b><br>When set to 1 the TX FIFO is almost empty and needs to be filled.                                                                                                          |
| 4   | irxffaull | <b>RX FIFO Almost Full.</b> When set to 1 the RX FIFO has met its almost full threshold and needs to be read by the microcontroller.                                                                       |
| 3   | iext      | <b>External Interrupt.</b><br>When set to 1 an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details. |
| 2   | ipksent   | <b>Packet Sent Interrupt.</b><br>When set to 1 a valid packet has been transmitted.                                                                                                                        |
| 1   | ipkvalid  | <b>Valid Packet Received.</b> When set to 1 a valid packet has been received.                                                                                                                              |
| 0   | icrcerror | <b>CRC Error.</b><br>When set to 1 the cyclic redundancy check is failed.                                                                                                                                  |

When any of the Interrupt/Status 1 bits change state from 0 to 1 the device will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 1 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 1 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

**Table 29. Interrupt or Status 1 Bit Set/Clear Description**

| Bit | Status Name | Set/Clear Conditions                                                                                                                                                                                                       |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ifferr      | Set if there is a FIFO overflow or underflow. Cleared by applying FIFO reset.                                                                                                                                              |
| 6   | itxffaull   | Set when the number of bytes written to TX FIFO is greater than the Almost Full threshold. Automatically cleared at the start of transmission when the number of bytes in the FIFO is less than or equal to the threshold. |
| 5   | itxffaem    | Set when the number of bytes in the TX FIFO is less than or equal to the Almost Empty threshold. Automatically cleared when the number of data bytes in the TX FIFO is above the Almost Empty threshold.                   |
| 4   | irxffaull   | Set when the number of bytes in the RX FIFO is greater than the Almost Full threshold. Cleared when the number of bytes in the RX FIFO is below the Almost Full threshold.                                                 |
| 3   | iext        | External interrupt source.                                                                                                                                                                                                 |
| 2   | ipksent     | Set once a packet is successfully sent (no TX abort). Cleared upon leaving FIFO mode or at the start of a new transmission.                                                                                                |
| 1   | ipkvalid    | Set up the successful reception of a packet (no RX abort). Cleared upon receiving and acknowledging the Sync Word for the next packet.                                                                                     |
| 0   | icrcerror   | Set if the CRC computed from the RX packet differs from the CRC in the TX packet. Cleared at the start of reception for the next packet.                                                                                   |

**Table 30. When are Individual Status Bits Set/Cleared if not Enabled as Interrupts?**

| Bit | Status Name | Set/Clear Conditions                                                                                                                                                                                                                                                                             |
|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | ifferr      | Set if there is a FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.                                                                                                                                                          |
| 6   | itxffaull   | Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).               |
| 5   | itxffaem    | Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold. |
| 4   | irxffaull   | Will be set when the number of bytes received (and not yet read-out) in RX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we read enough data from RX FIFO so that the number of data bytes not yet read is below the Almost Full threshold.        |
| 3   | iext        | External interrupt source                                                                                                                                                                                                                                                                        |
| 2   | ipksent     | Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.                                                                                                                       |
| 1   | ipkvalid    | Goes high once a packet is fully received (no RX abort). It is automatically cleaned once we receive and acknowledge the Sync Word for the next packet.                                                                                                                                          |
| 0   | icrcerror   | Goes High once the CRC computed during RX differs from the CRC sent in the packet by the TX. It is cleaned once we start receiving new data in the next packet.                                                                                                                                  |

**Register 04h. Interrupt/Status 2**

| Bit  | D7     | D6       | D5         | D4    | D3   | D2   | D1       | D0   |
|------|--------|----------|------------|-------|------|------|----------|------|
| Name | iswdet | ipreaval | ipreainval | irssi | iwut | ilbd | ichiprpy | ipor |
| Type | R      | R        | R          | R     | R    | R    | R        | R    |

Reset value = xxxxxxxx

| Bit | Name       | Function                                                                                                                                                                                                                         |
|-----|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | iswdet     | <b>Sync Word Detected.</b><br>When a sync word is detected this bit will be set to 1.                                                                                                                                            |
| 6   | ipreaval   | <b>Valid Preamble Detected.</b><br>When a preamble is detected this bit will be set to 1.                                                                                                                                        |
| 5   | ipreainval | <b>Invalid Preamble Detected.</b><br>When the preamble is not found within a period of time set by the invalid preamble detection threshold in Register 54h, this bit will be set to 1.                                          |
| 4   | irssi      | <b>RSSI.</b><br>When RSSI level exceeds the programmed threshold this bit will be set to 1.                                                                                                                                      |
| 3   | iwut       | <b>Wake-Up-Timer.</b><br>On the expiration of programmed wake-up timer this bit will be set to 1.                                                                                                                                |
| 2   | ilbd       | <b>Low Battery Detect.</b><br>When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. |
| 1   | ichiprpy   | <b>Chip Ready (XTAL).</b><br>When a chip ready event has been detected this bit will be set to 1.                                                                                                                                |
| 0   | ipor       | <b>Power-on-Reset (POR).</b><br>When the chip detects a Power on Reset above the desired setting this bit will be set to 1.                                                                                                      |

When any of the Interrupt/Status Register 2 bits change state from 0 to 1 the control block will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 2 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 2 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

**Table 31. Interrupt or Status 2 Bit Set/Clear Description**

| Bit | Status Name | Set/Clear Conditions                                                                                                                                                                                                                                                                |
|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | iswdet      | Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.                                                                                                                                                                                   |
| 6   | ipreaval    | Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.                                                                                                                                                                  |
| 5   | iprainval   | Self cleaning, user should use this as an interrupt source rather than a status.                                                                                                                                                                                                    |
| 4   | irssi       | Should remain high as long as the RSSI value is above programmed threshold level                                                                                                                                                                                                    |
| 3   | iwut        | Wake time timer interrupt. Use as an interrupt, not as a status.                                                                                                                                                                                                                    |
| 2   | ilbd        | Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced. |
| 1   | ichiprdy    | Chip ready goes high once we enable the xtal, TX or RX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.                                                                                                                         |
| 0   | ipor        | Power on status.                                                                                                                                                                                                                                                                    |

**Table 32. Detailed Description of Status Registers when not Enabled as Interrupts**

| Bit | Status Name | Set/Clear Conditions                                                                                                                                                                                                                                                                |
|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | iswdet      | Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.                                                                                                                                                                                   |
| 6   | ipreaval    | Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.                                                                                                                                                                  |
| 5   | iprainval   | Self cleaning, user should use this as an interrupt source rather than a status.                                                                                                                                                                                                    |
| 4   | irssi       | Should remain high as long as the RSSI value is above programmed threshold level                                                                                                                                                                                                    |
| 3   | iwut        | Wake time timer interrupt. Use as an interrupt, not as a status.                                                                                                                                                                                                                    |
| 2   | ilbd        | Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced. |
| 1   | ichiprdy    | Chip ready goes high once we enable the xtal, TX or RX, and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.                                                                                                                        |
| 0   | ipor        | Power on status.                                                                                                                                                                                                                                                                    |

**Register 05h. Interrupt Enable 1**

| Bit  | D7      | D6          | D5        | D4         | D3    | D2       | D1        | D0         |
|------|---------|-------------|-----------|------------|-------|----------|-----------|------------|
| Name | enfferr | entxffafull | entxffaem | enrxffaull | enext | enpksent | enpkvalid | encrcerror |
| Type | R/W     | R/W         | R/W       | R/W        | R/W   | R/W      | R/W       | R/W        |

Reset value = 00000000

| Bit | Name        | Function                                                                                                       |
|-----|-------------|----------------------------------------------------------------------------------------------------------------|
| 7   | enfferr     | <b>Enable FIFO Underflow/Overflow.</b><br>When set to 1 the FIFO Underflow/Overflow interrupt will be enabled. |
| 6   | entxffafull | <b>Enable TX FIFO Almost Full.</b><br>When set to 1 the TX FIFO Almost Full interrupt will be enabled.         |
| 5   | entxffaem   | <b>Enable TX FIFO Almost Empty.</b><br>When set to 1 the TX FIFO Almost Empty interrupt will be enabled.       |
| 4   | enrxffaull  | <b>Enable RX FIFO Almost Full.</b><br>When set to 1 the RX FIFO Almost Full interrupt will be enabled.         |
| 3   | enext       | <b>Enable External Interrupt.</b><br>When set to 1 the External Interrupt will be enabled.                     |
| 2   | enpksent    | <b>Enable Packet Sent.</b><br>When ipksent =1 the Packet Sense Interrupt will be enabled.                      |
| 1   | enpkvalid   | <b>Enable Valid Packet Received.</b><br>When ipkvalid = 1 the Valid Packet Received Interrupt will be enabled. |
| 0   | encrcerror  | <b>Enable CRC Error.</b><br>When set to 1 the CRC Error interrupt will be enabled.                             |

## Register 06h. Interrupt Enable 2

| Bit  | D7      | D6        | D5          | D4     | D3    | D2    | D1        | D0    |
|------|---------|-----------|-------------|--------|-------|-------|-----------|-------|
| Name | enswdet | enpreaval | enpreainval | enrssi | enwut | enlbd | enchiprdy | enpor |
| Type | R       | R         | R           | R      | R/W   | R/W   | R/W       | R/W   |

Reset value = 00000011

| Bit | Name        | Function                                                                                                              |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 7   | enswdet     | <b>Enable Sync Word Detected.</b><br>When mpreadet =1 the Preamble Detected Interrupt will be enabled.                |
| 6   | enpreaval   | <b>Enable Valid Preamble Detected.</b><br>When mpreadet =1 the Valid Preamble Detected Interrupt will be enabled.     |
| 5   | enpreainval | <b>Enable Invalid Preamble Detected.</b><br>When mpreadet =1 the Invalid Preamble Detected Interrupt will be enabled. |
| 4   | enrssi      | <b>Enable RSSI.</b><br>When set to 1 the RSSI Interrupt will be enabled.                                              |
| 3   | enwut       | <b>Enable Wake-Up Timer.</b><br>When set to 1 the Wake-Up Timer interrupt will be enabled.                            |
| 2   | enlbd       | <b>Enable Low Battery Detect.</b><br>When set to 1 the Low Battery Detect interrupt will be enabled.                  |
| 1   | enchiprdy   | <b>Enable Chip Ready (XTAL).</b><br>When set to 1 the Chip Ready interrupt will be enabled.                           |
| 0   | enpor       | <b>Enable POR.</b><br>When set to 1 the POR interrupt will be enabled.                                                |

**Register 07h. Operating Mode and Function Control 1**

| Bit  | D7    | D6    | D5   | D4      | D3   | D2   | D1    | D0   |
|------|-------|-------|------|---------|------|------|-------|------|
| Name | swres | enlbd | enwt | x32ksel | txon | rxon | pllon | xton |
| Type | R/W   | R/W   | R/W  | R/W     | R/W  | R/W  | R/W   | R/W  |

Reset value = 00000001

| Bit | Name    | Function                                                                                                                                                                                                                                                                                                                                    |
|-----|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | swres   | <b>Software Register Reset Bit.</b><br>This bit may be used to reset all registers simultaneously to a DEFAULT state, without the need for sequentially writing to each individual register. The RESET is accomplished by setting swres = 1. This bit will be automatically cleared.                                                        |
| 6   | enlbd   | <b>Enable Low Battery Detect.</b><br>When this bit is set to 1 the Low Battery Detector circuit and threshold comparison will be enabled.                                                                                                                                                                                                   |
| 5   | enwt    | <b>Enable Wake-Up-Timer.</b><br>Enabled when enwt = 1. If the Wake-up-Timer function is enabled it will operate in any mode and notify the microcontroller through the GPIO interrupt when the timer expires.                                                                                                                               |
| 4   | x32ksel | <b>32,768 kHz Crystal Oscillator Select.</b><br>0: RC oscillator<br>1: 32 kHz crystal                                                                                                                                                                                                                                                       |
| 3   | txon    | <b>TX on in Manual Transmit Mode.</b><br>Automatically cleared in FIFO mode once the packet is sent. Transmission can be aborted during packet transmission, however, when no data has been sent yet, transmission can only be aborted after the device is programmed to “unmodulated carrier” (“Register 71h. Modulation Mode Control 2”). |
| 2   | rxon    | <b>RX on in Manual Receiver Mode.</b><br>Automatically cleared if Multiple Packets config. is disabled and a valid packet received.                                                                                                                                                                                                         |
| 1   | pllon   | <b>TUNE Mode (PLL is ON).</b><br>When pllon = 1 the PLL will remain enabled in Idle State. This will for faster turn-around time at the cost of increased current consumption in Idle State.                                                                                                                                                |
| 0   | xton    | <b>READY Mode (Xtal is ON).</b>                                                                                                                                                                                                                                                                                                             |

## Register 08h. Operating Mode and Function Control 2

| Bit  | D7          | D6 | D5 | D4    | D3     | D2    | D1      | D0      |
|------|-------------|----|----|-------|--------|-------|---------|---------|
| Name | antdiv[2:0] |    |    | rxmpk | autotx | enldm | ffclrrx | ffclrtx |
| Type | R/W         |    |    | R/W   | R/W    | R/W   | R/W     | R/W     |

Reset value = 00000000

| Bit  | Name                               | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
|------|------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-------------|-----------------|--|--|--|-----------|-----------|-----------|-----------|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|---|---|---|---|------|-----------------------------|---|---|--|------|-----------------------------|---|---|--|------|------------------------------------|---|---|--|------|------------------------------------|---|---|--|
| 7:5  | antdiv[2:0]                        | <b>Enable Antenna Diversity.</b><br>The GPIO must be configured for Antenna Diversity for the algorithm to work properly. <table><thead><tr><th></th><th>RX/TX state</th><th colspan="3">non RX/TX state</th></tr><tr><th></th><th>GPIO Ant1</th><th>GPIO Ant2</th><th>GPIO Ant1</th><th>GPIO Ant2</th></tr></thead><tbody><tr><td>000:</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>001:</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>010:</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>011:</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>100:</td><td>antenna diversity algorithm</td><td>0</td><td>0</td><td></td></tr><tr><td>101:</td><td>antenna diversity algorithm</td><td>1</td><td>1</td><td></td></tr><tr><td>110:</td><td>ant. div. algorithm in beacon mode</td><td>0</td><td>0</td><td></td></tr><tr><td>111:</td><td>ant. div. algorithm in beacon mode</td><td>1</td><td>1</td><td></td></tr></tbody></table> |           | RX/TX state | non RX/TX state |  |  |  | GPIO Ant1 | GPIO Ant2 | GPIO Ant1 | GPIO Ant2 | 000: | 0 | 1 | 0 | 0 | 001: | 1 | 0 | 0 | 0 | 010: | 0 | 1 | 1 | 1 | 011: | 1 | 0 | 1 | 1 | 100: | antenna diversity algorithm | 0 | 0 |  | 101: | antenna diversity algorithm | 1 | 1 |  | 110: | ant. div. algorithm in beacon mode | 0 | 0 |  | 111: | ant. div. algorithm in beacon mode | 1 | 1 |  |
|      | RX/TX state                        | non RX/TX state                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
|      | GPIO Ant1                          | GPIO Ant2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | GPIO Ant1 | GPIO Ant2   |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 000: | 0                                  | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0         | 0           |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 001: | 1                                  | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0         | 0           |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 010: | 0                                  | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 1         | 1           |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 011: | 1                                  | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 1         | 1           |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 100: | antenna diversity algorithm        | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0         |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 101: | antenna diversity algorithm        | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 1         |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 110: | ant. div. algorithm in beacon mode | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 0         |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 111: | ant. div. algorithm in beacon mode | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 1         |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 4    | rxmpk                              | <b>RX Multi Packet.</b><br>When the chip is selected to use FIFO Mode (dtmod[1:0]) and RX Packet Handling (enpacrx) then it will fill up the FIFO with multiple valid packets if this bit is set, otherwise the transceiver will automatically leave the RX State after the first valid packet has been received.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 3    | autotx                             | <b>Automatic Transmission.</b><br>When autotx = 1 the transceiver will enter automatically TX State when the FIFO is almost full. When the FIFO is empty it will automatically return to the Idle State.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 2    | enldm                              | <b>Enable Low Duty Cycle Mode.</b><br>If this bit is set to 1 then the chip turns on the RX regularly. The frequency should be set in the Wake-Up Timer Period register, while the minimum ON time should be set in the Low-Duty Cycle Mode Duration register. The FIFO mode should be enabled also.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 1    | ffclrrx                            | <b>RX FIFO Reset/Clear.</b><br>This has to be a two writes operation: Setting ffclrrx =1 followed by ffclrrx = 0 will clear the contents of the RX FIFO.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |
| 0    | ffclrtx                            | <b>TX FIFO Reset/Clear.</b><br>This has to be a two writes operation: Setting ffclrtx =1 followed by ffclrtx = 0 will clear the contents of the TX FIFO.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |           |             |                 |  |  |  |           |           |           |           |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |   |   |   |   |      |                             |   |   |  |      |                             |   |   |  |      |                                    |   |   |  |      |                                    |   |   |  |

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**Register 09h. 30 MHz Crystal Oscillator Load Capacitance**


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| Bit         | D7       | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----|----|----|----|----|----|
| <b>Name</b> | xtalshft | xlc[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/W      | R/W      |    |    |    |    |    |    |

Reset value = 01111111

| Bit | Name     | Function                                                                                                      |
|-----|----------|---------------------------------------------------------------------------------------------------------------|
| 7   | xtalshft | Additional capacitance to course shift the frequency if xlc[6:0] is not sufficient. Not binary with xlc[6:0]. |
| 6:0 | xlc[6:0] | <b>Tuning Capacitance for the 30 MHz XTAL.</b>                                                                |

## Register 0Ah. Microcontroller Output Clock

| Bit  | D7       | D6 | D5        | D4 | D3    | D2        | D1 | D0 |
|------|----------|----|-----------|----|-------|-----------|----|----|
| Name | Reserved |    | clkt[1:0] |    | enlfc | mclk[2:0] |    |    |
| Type | R        |    | R/W       |    | R/W   | R/W       |    |    |

Reset value = xx000110

| Bit | Name      | Function                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved  | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:4 | clkt[1:0] | <b>Clock Tail.</b><br>If enlfc = 0 then it can be useful to provide a few extra cycles for the microcontroller to complete its operation. Setting the clkt[1:0] register will provide the addition cycles of the clock before it shuts off.<br>00: 0 cycle<br>01: 128 cycles<br>10: 256 cycles<br>11: 512 cycles                                                                                                                                  |
| 3   | enlfc     | <b>Enable Low Frequency Clock.</b><br>When enlfc = 1 and the chip is in Sleep mode then the 32.768 kHz clock will be provided to the microcontroller no matter what the selection of mclk[2:0] is. For example if mclk[2:0] = '000', 30 MHz will be available through the GPIO to output to the microcontroller in all Idle, TX, or RX states. When the chip is commanded to Sleep mode the 30 MHz clock will become 32.768 kHz.                  |
| 2:0 | mclk[2:0] | <b>Microcontroller Clock.</b><br>Different clock frequencies may be selected for configurable GPIO clock output. All clock frequencies are created by dividing the XTAL except for the 32 kHz clock which comes directly from the 32 kHz RC Oscillator. The mclk[2:0] setting is only valid when xton = 1 except the 111.<br>000: 30 MHz<br>001: 15 MHz<br>010: 10 MHz<br>011: 4 MHz<br>100: 3 MHz<br>101: 2 MHz<br>110: 1 MHz<br>111: 32.768 kHz |

**Register 0Bh. GPIO Configuration 0**

| Bit         | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|-------------|---------------|----|------|------------|----|----|----|----|
| <b>Name</b> | gpiodrv0[1:0] |    | pup0 | gpio0[4:0] |    |    |    |    |
| <b>Type</b> | R/W           |    | R/W  | R/W        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | gpiodrv0[1:0] | <b>GPIO Driving Capability Setting.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 5   | pup0          | <b>Pullup Resistor Enable on GPIO0.</b><br>When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 4:0 | gpio0[4:0]    | <b>GPIO0 pin Function Select.</b><br>00000: Power-On-Reset (output)<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: RX Data (output)<br>10101: RX State (output)<br>10110: RX FIFO Almost Full (output)<br>10111: Antenna 1 Switch used for antenna diversity (output)<br>11000: Antenna 2 Switch used for antenna diversity (output)<br>11001: Valid Preamble Detected (output)<br>11010: Invalid Preamble Detected (output)<br>11011: Sync Word Detected (output)<br>11100: Clear Channel Assessment (output)<br>11101: VDD<br>else : GND |

## Register 0Ch. GPIO Configuration 1

| Bit  | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|------|---------------|----|------|------------|----|----|----|----|
| Name | gpiodrv1[1:0] |    | pup1 | gpio1[4:0] |    |    |    |    |
| Type | R/W           |    | R/W  | R/W        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | gpiodrv1[1:0] | <b>GPIO Driving Capability Setting.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5   | pup1          | <b>Pullup Resistor Enable on GPIO1.</b><br>When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4:0 | gpio1[4:0]    | <b>GPIO1 pin Function Select.</b><br>00000: Inverted Power-On-Reset (output)<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: RX Data (output)<br>10101: RX State (output)<br>10110: RX FIFO Almost Full (output)<br>10111: Antenna 1 Switch used for antenna diversity (output)<br>11000: Antenna 2 Switch used for antenna diversity (output)<br>11001: Valid Preamble Detected (output)<br>11010: Invalid Preamble Detected (output)<br>11011: Sync Word Detected (output)<br>11100: Clear Channel Assessment (output)<br>11101: VDD<br>else : GND |

**Register 0Dh. GPIO Configuration 2**

| Bit         | D7            | D6 | D5   | D4         | D3 | D2 | D1 | D0 |
|-------------|---------------|----|------|------------|----|----|----|----|
| <b>Name</b> | gpiodrv2[1:0] |    | pup2 | gpio2[4:0] |    |    |    |    |
| <b>Type</b> | R/W           |    | R/W  | R/W        |    |    |    |    |

Reset value = 00000000

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | gpiodrv2[1:0] | <b>GPIO Driving Capability Setting.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 5   | pup2          | <b>Pullup Resistor Enable on GPIO2.</b><br>When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 4:0 | gpio2[4:0]    | <b>GPIO2 pin Function Select.</b><br>00000: Microcontroller Clock<br>00001: Wake-Up Timer: 1 when WUT has expired (output)<br>00010: Low Battery Detect: 1 when battery is below threshold setting (output)<br>00011: Direct Digital Input<br>00100: External Interrupt, falling edge (input)<br>00101: External Interrupt, rising edge (input)<br>00110: External Interrupt, state change (input)<br>00111: ADC Analog Input<br>01000: Reserved (Analog Test N Input)<br>01001: Reserved (Analog Test P Input)<br>01010: Direct Digital Output<br>01011: Reserved (Digital Test Output)<br>01100: Reserved (Analog Test N Output)<br>01101: Reserved (Analog Test P Output)<br>01110: Reference Voltage (output)<br>01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output)<br>10000: TX Data input for direct modulation (input)<br>10001: External Retransmission Request (input)<br>10010: TX State (output)<br>10011: TX FIFO Almost Full (output)<br>10100: RX Data (output)<br>10101: RX State (output)<br>10110: RX FIFO Almost Full (output)<br>10111: Antenna 1 Switch used for antenna diversity (output)<br>11000: Antenna 2 Switch used for antenna diversity (output)<br>11001: Valid Preamble Detected (output)<br>11010: Invalid Preamble Detected (output)<br>11011: Sync Word Detected (output)<br>11100: Clear Channel Assessment (output)<br>11101: VDD<br>else : GND |

## Register 0Eh. I/O Port Configuration

| Bit  | D7       | D6         | D5         | D4         | D3    | D2   | D1   | D0   |
|------|----------|------------|------------|------------|-------|------|------|------|
| Name | Reserved | extitst[2] | extitst[1] | extitst[0] | itsdo | dio2 | dio1 | dio0 |
| Type | R        | R          | R          | R          | R/W   | R/W  | R/W  | R/W  |

Reset value = 00000000

| Bit | Name       | Function                                                                                                                                                                                                                     |
|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved   | <b>Reserved.</b>                                                                                                                                                                                                             |
| 6   | extitst[2] | <b>External Interrupt Status.</b><br>If the GPIO2 is programmed to be external interrupt sources then the status can be read here.                                                                                           |
| 5   | extitst[1] | <b>External Interrupt Status.</b><br>If the GPIO1 is programmed to be external interrupt sources then the status can be read here.                                                                                           |
| 4   | extitst[0] | <b>External Interrupt Status.</b><br>If the GPIO0 is programmed to be external interrupt sources then the status can be read here.                                                                                           |
| 3   | itsdo      | <b>Interrupt Request Output on the SDO Pin.</b><br>nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).                                                                           |
| 2   | dio2       | <b>Direct I/O for GPIO2.</b><br>If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here. |
| 1   | dio1       | <b>Direct I/O for GPIO1.</b><br>If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here. |
| 0   | dio0       | <b>Direct I/O for GPIO0.</b><br>If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here. |

**Register 0Fh. ADC Configuration**

| Bit         | D7                   | D6          | D5 | D4 | D3          | D2 | D1           | D0 |
|-------------|----------------------|-------------|----|----|-------------|----|--------------|----|
| <b>Name</b> | adcstart/<br>adcdone | adcsel[2:0] |    |    | adcref[1:0] |    | adcgain[1:0] |    |
| <b>Type</b> | R/W                  | R/W         |    |    | R/W         |    | R/W          |    |

Reset value = 00000000

| Bit | Name             | Function                                                                                                                                                                                                                                                                                                                                                                |
|-----|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | adcstart/adcdone | <b>ADC Measurement Start Bit.</b><br>Reading this bit gives 1 if the ADC measurement cycle has been finished.                                                                                                                                                                                                                                                           |
| 6:4 | adcsel[2:0]      | <b>ADC Input Source Selection.</b><br>The internal 8-bit ADC input source can be selected as follows:<br>000: Internal Temperature Sensor<br>001: GPIO0, single-ended<br>010: GPIO1, single-ended<br>011: GPIO2, single-ended<br>100: GPIO0(+) – GPIO1(–), differential<br>101: GPIO1(+) – GPIO2(–), differential<br>110: GPIO0(+) – GPIO2(–), differential<br>111: GND |
| 3:2 | adcref[1:0]      | <b>ADC Reference Voltage Selection.</b><br>The reference voltage of the internal 8-bit ADC can be selected as follows:<br>0X: bandgap voltage (1.2 V)<br>10: VDD / 3<br>11: VDD / 2                                                                                                                                                                                     |
| 1:0 | adcgain[1:0]     | <b>ADC Sensor Amplifier Gain Selection.</b><br>The full scale range of the internal 8-bit ADC in differential mode (see adcsel) can be set as follows:<br>adcref[0] = 0: adcref[0] = 1:<br>$FS = 0.014 \times (adcgain[1:0] + 1) \times VDD$ $FS = 0.021 \times (adcgain[1:0] + 1) \times VDD$                                                                          |

## Register 10h. ADC Sensor Amplifier Offset

| Bit  | D7       | D6 | D5 | D4 | D3           | D2 | D1 | D0 |
|------|----------|----|----|----|--------------|----|----|----|
| Name | Reserved |    |    |    | adcoffs[3:0] |    |    |    |
| Type | R        |    |    |    | R/W          |    |    |    |

Reset value = xxxx0000

| Bit                                                                                                                                                  | Name         | Function                             |
|------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------------------------------|
| 7:4                                                                                                                                                  | Reserved     | <b>Reserved.</b>                     |
| 3:0                                                                                                                                                  | adcoffs[3:0] | <b>ADC Sensor Amplifier Offset*.</b> |
| <b>*Note:</b> The offset can be calculated as $\text{Offset} = \text{adcoffs}[2:0] \times \text{VDD} / 1000$ ; MSB = $\text{adcoffs}[3]$ = Sign bit. |              |                                      |

## Register 11h. ADC Value

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | adc[7:0] |    |    |    |    |    |    |    |
| Type | R        |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit | Name     | Function                                |
|-----|----------|-----------------------------------------|
| 7:0 | adc[7:0] | <b>Internal 8 bit ADC Output Value.</b> |

**Register 12h. Temperature Sensor Calibration**

| Bit         | D7           | D6 | D5       | D4       | D3          | D2 | D1 | D0 |
|-------------|--------------|----|----------|----------|-------------|----|----|----|
| <b>Name</b> | tsrange[1:0] |    | entsoffs | entstrim | tstrim[3:0] |    |    |    |
| <b>Type</b> | R/W          |    | R/W      | R/W      | R/W         |    |    |    |

Reset value = 00100000

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | tsrange[1:0] | <b>Temperature Sensor Range Selection.</b><br>(FS range is 0..1024 mV)<br>00:     −40 °C .. 64 °C (full operating range), with 0.5 °C resolution (1 LSB in the 8-bit ADC)<br>01:     −40 °C .. 85 °C, with 1 °C resolution (1 LSB in the 8-bit ADC)<br>11:     0 °C .. 85 °C, with 0.5 °C resolution (1 LSB in the 8-bit ADC)<br>10:     −40 °F .. 216 °F, with 1 °F resolution (1 LSB in the 8-bit ADC) |
| 5   | entsoffs     | <b>Temperature Sensor Offset to Convert from K to °C.</b>                                                                                                                                                                                                                                                                                                                                                |
| 4   | entstrim     | <b>Temperature Sensor Trim Enable.</b>                                                                                                                                                                                                                                                                                                                                                                   |
| 3:0 | tstrim[3:0]  | <b>Temperature Sensor Trim Value.</b>                                                                                                                                                                                                                                                                                                                                                                    |

**Register 13h. Temperature Value Offset**

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | tvoffs[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                                                                              |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------|
| 7:0 | tvoffs[7:0] | <b>Temperature Value Offset.</b><br>This value is added to the measured temperature value. (MSB, tvoffs[8]: sign bit) |

**Note:** If a new configuration is needed (e.g., for the WUT or the LDC), proper functionality is required. The function must first be disabled, then the settings changed, then enabled back on.

## Register 14h. Wake-Up Timer Period 1

| Bit  | D7       | D6 | D5 | D4       | D3 | D2  | D1 | D0 |
|------|----------|----|----|----------|----|-----|----|----|
| Name | Reserved |    |    | wtr[4:0] |    |     |    |    |
| Type | R/W      |    |    |          |    | R/W |    |    |

Reset value = xxx00011

| Bit                                                                                                                                                                                                                                                             | Name     | Function                                                                                                                                                                            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5                                                                                                                                                                                                                                                             | Reserved | <b>Reserved.</b>                                                                                                                                                                    |
| 4:0                                                                                                                                                                                                                                                             | wtr[4:0] | <b>Wake Up Timer Exponent (R) Value*.</b><br>Maximum value for R is decimal 20. A value greater than 20 will yield a result as if 20 were written. R Value = 0 can be written here. |
| <b>*Note:</b> The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768 \text{ ms}$ . R = 0 is allowed, and the maximum value for R is decimal 20. A value greater than 20 will result in the same as if 20 was written. |          |                                                                                                                                                                                     |

## Register 15h. Wake-Up Timer Period 2

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | wtm[15:8] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit                                                                                                                          | Name      | Function                                  |
|------------------------------------------------------------------------------------------------------------------------------|-----------|-------------------------------------------|
| 7:0                                                                                                                          | wtm[15:8] | <b>Wake Up Timer Mantissa (M) Value*.</b> |
| <b>*Note:</b> The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768 \text{ ms}$ . |           |                                           |

## Register 16h. Wake-Up Timer Period 3

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | wtm[7:0] |    |    |    |    |    |    |    |
| Type | R/W      |    |    |    |    |    |    |    |

Reset value = 00000001

| Bit                                                                                                                          | Name     | Function                                                                                             |
|------------------------------------------------------------------------------------------------------------------------------|----------|------------------------------------------------------------------------------------------------------|
| 7:0                                                                                                                          | wtm[7:0] | <b>Wake Up Timer Mantissa (M) Value*.</b><br>M[7:0] = 0 is not valid here. Write at least decimal 1. |
| <b>*Note:</b> The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768 \text{ ms}$ . |          |                                                                                                      |

**Register 17h. Wake-Up Timer Value 1**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | wtm[15:8] |    |    |    |    |    |    |    |
| Type | R         |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit                                                                                                                   | Name      | Function                                          |
|-----------------------------------------------------------------------------------------------------------------------|-----------|---------------------------------------------------|
| 7:0                                                                                                                   | wtm[15:8] | <b>Wake Up Timer Current Mantissa (M) Value*.</b> |
| *Note: The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768 \text{ ms}$ . |           |                                                   |

**Register 18h. Wake-Up Timer Value 2**

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | wtm[7:0] |    |    |    |    |    |    |    |
| Type | R        |    |    |    |    |    |    |    |

Reset value = xxxxxxxx

| Bit                                                                                                                   | Name     | Function                                          |
|-----------------------------------------------------------------------------------------------------------------------|----------|---------------------------------------------------|
| 7:0                                                                                                                   | wtm[7:0] | <b>Wake Up Timer Current Mantissa (M) Value*.</b> |
| *Note: The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R) / 32.768 \text{ ms}$ . |          |                                                   |

**Register 19h. Low-Duty Cycle Mode Duration**

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | ldc[7:0] |    |    |    |    |    |    |    |
| Type | R/W      |    |    |    |    |    |    |    |

Reset value = 00000001

| Bit                                                                                                                                                                                                                           | Name     | Function                                                                                                                                                                                                                                                                                                                                                                                               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0                                                                                                                                                                                                                           | ldc[7:0] | <b>Low-Duty Cycle Mode Duration (LDC)*.</b><br>If enabled, the LDC will start together when the WUT is supposed to start, and the duration of the LDC is specified by the address 19h and the equation that goes with it. In order for the LDC to work, the LDC value has to be smaller than the M value specified in registers 15h and 16h.<br>LDC = 0 is not allowed here. Write at least decimal 1. |
| *Note: The period of the low-duty cycle ON time can be calculated as $T_{LDC\_ON} = (4 \times LDC \times 2^R) / 32.768 \text{ ms}$ . R is the same as in the wake-up timer setting in "Register 14h. Wake-Up Timer Period 1". |          |                                                                                                                                                                                                                                                                                                                                                                                                        |

## Register 1Ah. Low Battery Detector Threshold

| Bit  | D7       | D6 | D5 | D4       | D3 | D2 | D1 | D0 |
|------|----------|----|----|----------|----|----|----|----|
| Name | Reserved |    |    | lbd[4:0] |    |    |    |    |
| Type | R        |    |    | R/W      |    |    |    |    |

Reset value = xxx10100

| Bit                                                                                                        | Name     | Function                                                                                                                                                                                             |
|------------------------------------------------------------------------------------------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5                                                                                                        | Reserved | <b>Reserved.</b>                                                                                                                                                                                     |
| 4:0                                                                                                        | lbd[4:0] | <b>Low Battery Detector Threshold.</b><br>This threshold is compared to Battery Voltage Level. If the Battery Voltage is less than the threshold the Low Battery Interrupt is set. Default = 2.7 V.* |
| *Note: The threshold can be calculated as $V_{\text{threshold}} = 1.7 + \text{lbd} \times 50 \text{ mV}$ . |          |                                                                                                                                                                                                      |

## Register 1Bh. Battery Voltage Level

| Bit  | D7       | D6 | D5 | D4        | D3 | D2 | D1 | D0 |
|------|----------|----|----|-----------|----|----|----|----|
| Name | Reserved |    |    | vbat[4:0] |    |    |    |    |
| Type | R        |    |    | R         |    |    |    |    |

Reset value = xxxxxxxx

| Bit | Name      | Function                                                                                                                                                                        |
|-----|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Reserved  | <b>Reserved.</b>                                                                                                                                                                |
| 4:0 | vbat[4:0] | <b>Battery Voltage Level.</b><br>The battery voltage is converted by a 5 bit ADC. In Sleep Mode the register is updated in every 1 s. In other states it measures continuously. |

**Register 1Ch. IF Filter Bandwidth**

| Bit         | D7          | D6            | D5 | D4 | D3          | D2 | D1 | D0 |
|-------------|-------------|---------------|----|----|-------------|----|----|----|
| <b>Name</b> | dwn3_bypass | ndec_exp[2:0] |    |    | filset[3:0] |    |    |    |
| <b>Type</b> | R/W         | R/W           |    |    | R/W         |    |    |    |

Reset value = 00000001

| Bit | Name          | Function                                                                                            |
|-----|---------------|-----------------------------------------------------------------------------------------------------|
| 7   | dwn3_bypass   | <b>Bypass Decimator by 3 (if set).</b>                                                              |
| 6:4 | ndec_exp[2:0] | <b>IF Filter Decimation Rates.</b>                                                                  |
| 3:0 | filset[3:0]   | <b>IF Filter Coefficient Sets.</b><br>Defaults are for Rb = 40 kbps and Fd = 20 kHz so Bw = 80 kHz. |

**Register 1Dh. AFC Loop Gearshift Override**

| Bit         | D7    | D6     | D5            | D4 | D3 | D2            | D1 | D0 |
|-------------|-------|--------|---------------|----|----|---------------|----|----|
| <b>Name</b> | afcbd | enaafc | afcgearh[2:0] |    |    | afcgearl[2:0] |    |    |
| <b>Type</b> | R/W   | R/W    | R/W           |    |    | R/W           |    |    |

Reset value = 01000000

| Bit | Name          | Function                                                         |
|-----|---------------|------------------------------------------------------------------|
| 7   | afcbd         | <b>If set, the tolerated AFC frequency error will be halved.</b> |
| 6   | enaafc        | <b>AFC Enable.</b>                                               |
| 5:3 | afcgearh[2:0] | <b>AFC High Gear Setting.</b>                                    |
| 2:0 | afcgearl[2:0] | <b>AFC Low Gear Setting.</b>                                     |

## Register 1Eh. AFC Timing Control

| Bit  | D7       | D6 | D5          | D4 | D3 | D2          | D1 | D0 |
|------|----------|----|-------------|----|----|-------------|----|----|
| Name | Reserved |    | shwait[2:0] |    |    | anwait[2:0] |    |    |
| Type | R        |    | R/W         |    |    | R/W         |    |    |

Reset value = xx001010

| Bit | Name        | Function                                                                                                                                                                                                                                 |
|-----|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved    | <b>Reserved.</b>                                                                                                                                                                                                                         |
| 5:3 | shwait[2:0] | <b>Short Wait Periods after AFC Correction.</b><br>Used before preamble is detected. Short wait = $(\text{RegValue} + 1) \times 2T_b$ . If set to 0 then no AFC correction will occur before preamble detect, i.e. AFC will be disabled. |
| 2:0 | anwait[2:0] | <b>Antenna Switching Wait Time.</b><br>Value corresponds to number of bits.                                                                                                                                                              |

**Register 1Fh. Clock Recovery Gearshift Override**

| Bit         | D7       | D6      | D5          | D4 | D3 | D2          | D1 | D0 |
|-------------|----------|---------|-------------|----|----|-------------|----|----|
| <b>Name</b> | Reserved | rxready | crfast[2:0] |    |    | crslow[2:0] |    |    |
| <b>Type</b> | R/W      | R/W     | R/W         |    |    | R/W         |    |    |

Reset value = 00000011

| Bit | Name        | Function                                                                                                                                                                                                                        |
|-----|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved    | <b>Reserved.</b>                                                                                                                                                                                                                |
| 6   | rxready     | <b>Improves Receiver Noise Immunity when in Direct Mode.</b><br>It is recommended to set this bit after preamble is detected. When in FIFO mode this bit should be set to “0” since noise immunity is controlled automatically. |
| 5:3 | crfast[2:0] | <b>Clock Recovery Fast Gearshift Value.</b>                                                                                                                                                                                     |
| 2:0 | crslow[2:0] | <b>Clock Recovery Slow Gearshift Value.</b>                                                                                                                                                                                     |

The gear-shift register controls BCR loop gain. Before the preamble is detected, BCR loop gain is as follows:

$$BCRLoopGain = \frac{crgain}{2^{crfast}}$$

Once the preamble is detected, internal state machine automatically shift BCR loop gain to the following:

$$BCRLoopGain = \frac{crgain}{2^{crslow}}$$

crfast = 3'b000 and crslow = 3'b101 are recommended for most applications. The value of “crslow” should be greater than “crfast”.

**Register 20h. Clock Recovery Oversampling Rate**

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | rxosr[7:0] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 01100100

| Bit | Name       | Function                                                                                                   |
|-----|------------|------------------------------------------------------------------------------------------------------------|
| 7:0 | rxosr[7:0] | <b>Oversampling Rate.</b><br>3 LSBs are the fraction, default = 0110 0100 = 12.5 clock cycles per data bit |

The oversampling rate can be calculated as  $rxosr = 500 \text{ kHz} / (2^{ndec\_exp} \times RX\_DR)$ . The *ndec\_exp* and the *dwn3\_bypass* values found at Address: 1Ch – IF Filter Bandwidth register together with the receive data rate (*Rb*) are the parameters needed to calculate *rxosr*:

$$rxosr = \frac{500 \times (1 + 2 \times dwn3\_bypass)}{2^{ndec\_exp-3} \times Rb \times (1 + enmanch)}$$

The *Rb* unit used in this equation is in kbps. The *enmanch* is the Manchester Coding parameter (see Reg. 70h, *enmach* is 1 when Manchester coding is enabled, *enmanch* is 0 when disabled). The number found in the equation should be rounded to an integer. The integer can be translated to a hexadecimal.

For optimal modem performance it is recommended to set the *rxosr* to at least 8. A higher *rxosr* can be obtained by choosing a lower value for *ndec\_exp* or enable *dwn3\_bypass*. A correction in *filset* might be needed to correct the channel select bandwidth to the desired value. Note that when *ndec\_exp* or *dwn3\_bypass* are changed the related parameters (*rxosr*, *ncoff* and *crgain*) need to be updated.

**Register 21h. Clock Recovery Offset 2**

| Bit  | D7          | D6 | D5 | D4        | D3           | D2 | D1 | D0 |
|------|-------------|----|----|-----------|--------------|----|----|----|
| Name | rxosr[10:8] |    |    | stallctrl | ncoff[19:16] |    |    |    |
| Type | R/W         |    |    | R/W       | R/W          |    |    |    |

Reset value = 00000001

| Bit | Name         | Function                                 |
|-----|--------------|------------------------------------------|
| 7:5 | rxosr[10:8]  | <b>Oversampling Rate.</b><br>Upper bits. |
| 4   | stallctrl    | <b>Used for BCR Purposes.</b>            |
| 3:0 | ncoff[19:16] | <b>NCO Offset.</b><br>See formula above. |

The offset can be calculated as follows:

$$ncoff = \frac{Rb \times (1 + enmanch) \times 2^{20+ndec\_exp}}{500 \times (1 + 2 \times dwn3\_bypass)}$$

The default values for register 20h to 23h gives 40 kbps RX\_DR with Manchester coding is disenabled.

**Register 22h. Clock Recovery Offset 1**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | ncoff[15:8] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 01000111

| Bit | Name        | Function                                |
|-----|-------------|-----------------------------------------|
| 7:0 | ncoff[15:8] | <b>NCO Offset.</b><br>See formula above |

**Register 23h. Clock Recovery Offset 0**

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | ncoff[7:0] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 10101110

| Bit | Name       | Function                                |
|-----|------------|-----------------------------------------|
| 7:0 | ncoff[7:0] | <b>NCO Offset.</b><br>See formula above |

**Register 24h. Clock Recovery Timing Loop Gain 1**

| Bit  | D7       | D6 | D5 | D4 | D3 | D2           | D1 | D0 |
|------|----------|----|----|----|----|--------------|----|----|
| Name | Reserved |    |    |    |    | crgain[10:8] |    |    |
| Type | R/W      |    |    |    |    | R/W          |    |    |

Reset value = 00000010

| Bit | Name         | Function                                |
|-----|--------------|-----------------------------------------|
| 7:3 | Reserved     | <b>Reserved.</b>                        |
| 2:0 | crgain[10:8] | <b>Clock Recovery Timing Loop Gain.</b> |

The loop gain can be calculated as follows:

$$\text{crgain} = 2 + \frac{2^{15} \times (1 + \text{enmanch}) \times \text{Rb}}{\text{rxosr} \times \text{Fd}}$$

**Register 25h. Clock Recovery Timing Loop Gain 0**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | crgain[7:0] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 10001111

| Bit | Name        | Function                                |
|-----|-------------|-----------------------------------------|
| 7:0 | crgain[7:0] | <b>Clock Recovery Timing Loop Gain.</b> |

**Register 26h. Received Signal Strength Indicator**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | rssi[7:0] |    |    |    |    |    |    |    |
| Type | R         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                  |
|-----|-----------|-------------------------------------------|
| 7:0 | rssi[7:0] | Received Signal Strength Indicator Value. |

**Register 27h. RSSI Threshold for Clear Channel Indicator**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | rssith[7:0] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00011110

| Bit | Name        | Function                                                                              |
|-----|-------------|---------------------------------------------------------------------------------------|
| 7:0 | rssith[7:0] | <b>RSSI Threshold.</b><br>Interrupt is set if the RSSI value is above this threshold. |

**Register 28h. Antenna Diversity 1**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | adrssi[7:0] |    |    |    |    |    |    |    |
| Type | R           |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                          |
|-----|-------------|-----------------------------------|
| 7:0 | adrssi[7:0] | Measured RSSI Value on Antenna 1. |

## Register 29h. Antenna Diversity 2

| Bit  | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | adrssi2[7:0] |    |    |    |    |    |    |    |
| Type | R            |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name         | Function                          |
|-----|--------------|-----------------------------------|
| 7:0 | adrssi2[7:0] | Measured RSSI Value on Antenna 2. |

## Register 2Ah. AFC Limiter

| Bit  | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | Afcclim[7:0] |    |    |    |    |    |    |    |
| Type | R/W          |    |    |    |    |    |    |    |

Reset value = 00101010

| Bit | Name         | Function                                  |
|-----|--------------|-------------------------------------------|
| 7:0 | Afcclim[7:0] | <b>AFC Limiter.</b><br>AFC limiter value. |

For the following registers (addresses 2Bh and 2Ch), use the following equation:

$$ook\_cnt\_val = \frac{3 \times 500[\text{kHz}]}{R_b \times (enmanch + 1)}$$

where  $R_b$ 's unit is in kHz and "enmanch" is the Manchester Enable bit (found at address 71h bit [1]).

Therefore, the minimal data rate that this register can support without Manchester is 0.366 kbps.

## Register 2Bh. AFC Correction (LSBs)

| Bit  | D7            | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|
| Name | afc_corr[9:2] |    |    |    |    |    |    |    |
| Type | R             |    |    |    |    |    |    |    |

Reset value = 00101011

| Bit | Name          | Function                                                                                                                                                                 |
|-----|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | afc_corr[9:2] | <b>AFC Correction Values.</b><br>AFC loop correction values [9:2] (MSBs only). Values are updated once, after sync word is found during receiving. See also address 2Ch. |

**Register 2Ch. OOK Counter Value 1**

| Bit         | D7            | D6 | D5       | D4        | D3      | D2         | D1        | D0        |
|-------------|---------------|----|----------|-----------|---------|------------|-----------|-----------|
| <b>Name</b> | afc_corr[1:0] |    | ookfrzen | peakdeten | madeten | ookcnt[10] | ookcnt[9] | ookcnt[8] |
| <b>Type</b> | R             |    | R/W      | R/W       | R/W     | R/W        | R/W       | R/W       |

Reset value = 00101100

| Bit | Name          | Function                                                                                                                                                            |
|-----|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | afc_corr[1:0] | <b>AFC Correction Values.</b><br>AFC loop correction values [1:0] (LSBs). Values are updated once, after sync word is found during receiving. See also address 2Bh. |
| 5   | ookfrzen      | <b>OOK Freeze.</b><br>OOK AGC freeze if this bit is set.                                                                                                            |
| 4   | peakdeten     | <b>Peak Detector Enable.</b><br>Peak detector enable if high.                                                                                                       |
| 3   | madeten       | <b>MA_Enable.</b><br>MA block enable if high.                                                                                                                       |
| 2:0 | ookcnt[2:0]   | <b>OOK Counter [10:8].</b><br>OOK counter value MSBs.                                                                                                               |

**Register 2Dh. OOK Counter Value 2**

| Bit         | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----|----|----|----|----|
| <b>Name</b> | ookcnt[7:0] |    |    |    |    |    |    |    |
| <b>Type</b> | R/W         |    |    |    |    |    |    |    |

Reset value = 00101101

| Bit | Name          | Function                                             |
|-----|---------------|------------------------------------------------------|
| 7:0 | afc_corr[9:2] | <b>OOK Counter [7:0].</b><br>OOK counter value LSBs. |

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**Register 2Eh. Slicer Peak Holder**

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| Bit         | D7       | D6          | D5 | D4 | D3         | D2 | D1 | D0 |
|-------------|----------|-------------|----|----|------------|----|----|----|
| <b>Name</b> | Reserved | attack[2:0] |    |    | decay[3:0] |    |    |    |
| <b>Type</b> | R/W      | R/W         |    |    | R/W        |    |    |    |

Reset value = 00101110

| Bit | Name        | Function         |
|-----|-------------|------------------|
| 7   | Reserved    | <b>Reserved.</b> |
| 6:4 | attack[2:0] | <b>Attack.</b>   |
| 3:0 | decay[3:0]  | <b>Decay.</b>    |

**Register 30h. Data Access Control**

| Bit         | D7      | D6      | D5       | D4       | D3      | D2    | D1       | D0 |
|-------------|---------|---------|----------|----------|---------|-------|----------|----|
| <b>Name</b> | enpacrx | lsbfrst | crcdonly | Reserved | enpactx | encrc | crc[1:0] |    |
| <b>Type</b> | R/W     | R/W     | R/W      | R/W      | R/W     | R/W   | R/W      |    |

Reset value = 10001101

| Bit | Name     | Function                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | enpacrx  | <b>Enable Packet RX Handling.</b><br>If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpacrx = 1 will enable automatic packet handling in the RX path. Register 30–4D allow for various configurations of the packet structure. Setting enpacrx = 0 will not do any packet handling in the RX path. It will only receive everything after the sync word and fill up the RX FIFO. |
| 6   | lsbfrst  | <b>LSB First Enable.</b><br>The LSB of the data will be transmitted/received first if this bit is set.                                                                                                                                                                                                                                                                                                                     |
| 5   | crcdonly | <b>CRC Data Only Enable.</b><br>When this bit is set to 1 the CRC is calculated on and checked against the packet data fields only.                                                                                                                                                                                                                                                                                        |
| 4   | Reserved | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3   | enpactx  | <b>Enable Packet TX Handling.</b><br>If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpactx = 1 will enable automatic packet handling in the TX path. Register 30–4D allow for various configurations of the packet structure. Setting enpactx = 0 will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO.                            |
| 2   | encrc    | <b>CRC Enable.</b><br>Cyclic Redundancy Check generation is enabled if this bit is set.                                                                                                                                                                                                                                                                                                                                    |
| 1:0 | crc[1:0] | <b>CRC Polynomial Selection.</b><br>00: CCITT<br>01: CRC-16 (IBM)<br>10: IEC-16<br>11: Biacheva                                                                                                                                                                                                                                                                                                                            |

Register 31h. EZMAC<sup>®</sup> Status

| Bit  | D7       | D6     | D5      | D4   | D3      | D2       | D1   | D0     |
|------|----------|--------|---------|------|---------|----------|------|--------|
| Name | Reserved | rxcrc1 | pksrcch | pkrx | pkvalid | crcerror | pktx | pksent |
| Type | R        | R      | R       | R    | R       | R        | R    | R      |

Reset value = 00000000

| Bit | Name     | Function                                                                                                                                                                  |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved | <b>Reserved.</b>                                                                                                                                                          |
| 6   | rxcrc1   | <b>If high, it indicates the last CRC received is all one's.</b><br>May indicated Transmitter underflow in case of CRC error.                                             |
| 5   | pksrcch  | <b>Packet Searching.</b><br>When pksrcch = 1 the radio is searching for a valid packet.                                                                                   |
| 4   | pkrx     | <b>Packet Receiving.</b><br>When pkrx = 1 the radio is currently receiving a valid packet.                                                                                |
| 3   | pkvalid  | <b>Valid Packet Received.</b><br>When a pkvalid = 1 a valid packet has been received by the receiver. (Same bit as in register 03, but reading it does not reset the IRQ) |
| 2   | crcerror | <b>CRC Error.</b><br>When crcerror = 1 a Cyclic Redundancy Check error has been detected. (Same bit as in register 03, but reading it does not reset the IRQ)             |
| 1   | pktx     | <b>Packet Transmitting.</b><br>When pktx = 1 the radio is currently transmitting a packet.                                                                                |
| 0   | pksent   | <b>Packet Sent.</b><br>A pksent = 1 a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ)                              |

## Register 32h. Header Control 1

| Bit  | D7        | D6 | D5 | D4 | D3        | D2 | D1 | D0 |
|------|-----------|----|----|----|-----------|----|----|----|
| Name | bcen[3:0] |    |    |    | hdch[3:0] |    |    |    |
| Type | R/W       |    |    |    | R/W       |    |    |    |

Reset value = 00001100

| Bit | Name      | Function                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | bcen[3:0] | <b>Broadcast Address (FFh) Check Enable.</b><br>If it is enabled together with Header Byte Check then the header check is OK if the incoming header byte equals with the appropriate check byte or FFh). One hot encoding.<br>0000: No broadcast address enable.<br>0001: Broadcast address enable for header byte 0.<br>0010: Broadcast address enable for header byte 1.<br>0011: Broadcast address enable for header bytes 0 & 1.<br>0100: ... |
| 3:0 | hdch[3:0] | <b>Received Header Bytes to be Checked Against the Check Header Bytes.</b><br>One hot encoding. The receiver will use hdch[2:0] to know the position of the Header Bytes.<br>0000: No Received Header check<br>0001: Received Header check for byte 0.<br>0010: Received Header check for bytes 1.<br>0011: Received header check for bytes 0 & 1.<br>0100: ...                                                                                   |

## Register 33h. Header Control 2

| Bit         | D7       | D6         | D5 | D4 | D3       | D2            | D1 | D0         |
|-------------|----------|------------|----|----|----------|---------------|----|------------|
| <b>Name</b> | Reserved | hdlen[2:0] |    |    | fixpklen | syncnlen[1:0] |    | prealen[8] |
| <b>Type</b> | R        | R/W        |    |    | R/W      | R/W           |    | R/W        |

Reset value = 00100010

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                                               |
|-----|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved      | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                       |
| 6:4 | hdlen[2:0]    | <b>Header Length.</b><br>Length of header used if packet handler is enabled for TX/RX (enpactx/rx). Headers are transmitted/received in descending order.<br>000: No TX/RX header<br>001: Header 3<br>010: Header 3 and 2<br>011: Header 3 and 2 and 1<br>100: Header 3 and 2 and 1 and 0                                                                              |
| 3   | fixpklen      | <b>Fix Packet Length.</b><br>When fixpklen = 1 the packet length (pklen[7:0]) is not included in the header. When fixpklen = 0 the packet length is included in the header.                                                                                                                                                                                            |
| 2:1 | syncnlen[1:0] | <b>Synchronization Word Length.</b><br>The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted in descending order.<br>00: Synchronization Word 3<br>01: Synchronization Word 3 and 2<br>10: Synchronization Word 3 and 2 and 1<br>11: Synchronization Word 3 and 2 and 1 and 0 |
| 0   | prealen[8]    | <b>MSB of Preamble Length.</b><br>See register Preamble Length.                                                                                                                                                                                                                                                                                                        |

**Register 34h. Preamble Length**

| Bit  | D7           | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------|----|----|----|----|----|----|----|
| Name | prealen[7:0] |    |    |    |    |    |    |    |
| Type | R/W          |    |    |    |    |    |    |    |

Reset value = 00001000

| Bit | Name         | Function                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | prealen[7:0] | <b>Preamble Length.</b><br>The value in the prealen[8:0] register corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '000001000' corresponds to a preamble length of 32 bits (8 x 4bits) or 4 bytes. The maximum preamble length is prealen[8:0] = 11111111 which corresponds to a 255 bytes Preamble. Writing 0 will have the same result as if writing 1, which corresponds to one single nibble of preamble. |

**Register 35h. Preamble Detection Control 1**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2               | D1 | D0 |
|------|-------------|----|----|----|----|------------------|----|----|
| Name | preath[4:0] |    |    |    |    | rssi_offset[2:0] |    |    |
| Type | R/W         |    |    |    |    | R/W              |    |    |

Reset value = 00101010

| Bit | Name             | Function                                                                                                                                             |
|-----|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | preath[4:0]      | <b>Number of nibbles processed during detection.</b>                                                                                                 |
| 2:0 | rssi_offset[2:0] | <b>rssi_offset[2:0]</b><br>Value added as offset to RSSI calculation. Every increment in this register results in an increment of +4 dB in the RSSI. |

## Register 36h. Synchronization Word 3

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | sync[31:24] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00101101

| Bit | Name        | Function                                                                            |
|-----|-------------|-------------------------------------------------------------------------------------|
| 7:0 | sync[31:24] | <b>Synchronization Word 3.</b><br>4 <sup>th</sup> byte of the synchronization word. |

## Register 37h. Synchronization Word 2

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | sync[23:16] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 11010100

| Bit | Name        | Function                                                                            |
|-----|-------------|-------------------------------------------------------------------------------------|
| 7:0 | sync[23:16] | <b>Synchronization Word 2.</b><br>3 <sup>rd</sup> byte of the synchronization word. |

## Register 38h. Synchronization Word 1

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | sync[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                                            |
|-----|------------|-------------------------------------------------------------------------------------|
| 7:0 | sync[15:8] | <b>Synchronization Word 1.</b><br>2 <sup>nd</sup> byte of the synchronization word. |

**Register 39h. Synchronization Word 0**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | sync[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                                                            |
|-----|-----------|-------------------------------------------------------------------------------------|
| 7:0 | sync[7:0] | <b>Synchronization Word 0.</b><br>1 <sup>st</sup> byte of the synchronization word. |

**Register 3Ah. Transmit Header 3**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | txhd[31:24] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                                           |
|-----|-------------|------------------------------------------------------------------------------------|
| 7:0 | txhd[31:24] | <b>Transmit Header 3.</b><br>4 <sup>th</sup> byte of the header to be transmitted. |

**Register 3Bh. Transmit Header 2**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | txhd[23:16] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                                           |
|-----|-------------|------------------------------------------------------------------------------------|
| 7:0 | txhd[23:16] | <b>Transmit Header 2.</b><br>3 <sup>rd</sup> byte of the header to be transmitted. |

## Register 3Ch. Transmit Header 1

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | txhd[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                                           |
|-----|------------|------------------------------------------------------------------------------------|
| 7:0 | txhd[15:8] | <b>Transmit Header 1.</b><br>2 <sup>nd</sup> byte of the header to be transmitted. |

## Register 3Dh. Transmit Header 0

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | txhd[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                                                           |
|-----|-----------|------------------------------------------------------------------------------------|
| 7:0 | txhd[7:0] | <b>Transmit Header 0.</b><br>1 <sup>st</sup> byte of the header to be transmitted. |

## Register 3Eh. Packet Length

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | pklen[7:0] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | pklen[7:0] | <b>Packet Length.</b><br>The value in the pklen[7:0] register corresponds directly to the number of bytes in the Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. Writing 0 is possible, in this case we do not send any data in the packet. During RX, if <i>fixpklen</i> = 1, this will specify also the Packet Length for RX mode. |

Check Header bytes 3 to 0 are checked against the corresponding bytes in the Received Header if the check is enabled in "Register 31h. EZMAC<sup>®</sup> Status," on page 116.

**Register 3Fh. Check Header 3**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | chhd[31:24] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                            |
|-----|-------------|---------------------------------------------------------------------|
| 7:0 | chhd[31:24] | <b>Check Header 3.</b><br>4 <sup>th</sup> byte of the check header. |

**Register 40h. Check Header 2**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | chhd[23:16] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                            |
|-----|-------------|---------------------------------------------------------------------|
| 7:0 | chhd[23:16] | <b>Check Header 2.</b><br>3 <sup>rd</sup> byte of the check header. |

**Register 41h. Check Header 1**

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | chhd[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                            |
|-----|------------|---------------------------------------------------------------------|
| 7:0 | chhd[15:8] | <b>Check Header 1.</b><br>2 <sup>nd</sup> byte of the check header. |

## Register 42h. Check Header 0

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | chhd[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                                            |
|-----|-----------|---------------------------------------------------------------------|
| 7:0 | chhd[7:0] | <b>Check Header 0.</b><br>1 <sup>st</sup> byte of the check header. |

Header Enable bytes 3 to 0 control which bits of the Check Header bytes are checked against the corresponding bits in the Received Header. Only those bits are compared where the enable bits are set to 1.

## Register 43h. Header Enable 3

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | hden[31:24] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                             |
|-----|-------------|----------------------------------------------------------------------|
| 7:0 | hden[31:24] | <b>Header Enable 3.</b><br>4 <sup>th</sup> byte of the check header. |

## Register 44h. Header Enable 2

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | hden[23:16] |    |    |    |    |    |    |    |
| Type | R/W         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                             |
|-----|-------------|----------------------------------------------------------------------|
| 7:0 | hden[23:16] | <b>Header Enable 2.</b><br>3 <sup>rd</sup> byte of the check header. |

**Register 45h. Header Enable 1**

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | hden[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                             |
|-----|------------|----------------------------------------------------------------------|
| 7:0 | hden[15:8] | <b>Header Enable 1.</b><br>2 <sup>nd</sup> byte of the check header. |

**Register 46h. Header Enable 0**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | hden[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                                             |
|-----|-----------|----------------------------------------------------------------------|
| 7:0 | hden[7:0] | <b>Header Enable 0.</b><br>1 <sup>st</sup> byte of the check header. |

**Register 47h. Received Header 3**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | rxhd[31:24] |    |    |    |    |    |    |    |
| Type | R           |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                                  |
|-----|-------------|---------------------------------------------------------------------------|
| 7:0 | rxhd[31:24] | <b>Received Header 3.</b><br>4 <sup>th</sup> byte of the received header. |

---

**Register 48h. Received Header 2**

---

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | rxhd[23:16] |    |    |    |    |    |    |    |
| Type | R           |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name        | Function                                                                  |
|-----|-------------|---------------------------------------------------------------------------|
| 7:0 | rxhd[23:16] | <b>Received Header 2.</b><br>3 <sup>rd</sup> byte of the received header. |

---

**Register 49h. Received Header 1**

---

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | rxhd[15:8] |    |    |    |    |    |    |    |
| Type | R          |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name       | Function                                                                  |
|-----|------------|---------------------------------------------------------------------------|
| 7:0 | rxhd[15:8] | <b>Received Header 1.</b><br>2 <sup>nd</sup> byte of the received header. |

---

**Register 4Ah. Received Header 0**

---

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | rxhd[7:0] |    |    |    |    |    |    |    |
| Type | R         |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                                                                  |
|-----|-----------|---------------------------------------------------------------------------|
| 7:0 | rxhd[7:0] | <b>Received Header 0.</b><br>1 <sup>st</sup> byte of the received header. |

**Register 4Bh. Received Packet Length**

| Bit  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-------------|----|----|----|----|----|----|----|
| Name | rxplen[7:0] |    |    |    |    |    |    |    |
| Type | R           |    |    |    |    |    |    |    |

Reset value = 11111111

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | rxplen[7:0] | <b>Length Byte of the Received Packet during <i>fixpklen</i> = 0.</b><br>(Specifies the number of Data bytes in the last received packet) This will be relevant ONLY if <i>fixpklen</i> (address 33h, bit[3]) is low during the receive time. If <i>fixpklen</i> is high, then the number of received Data Bytes can be read from the <i>pklen</i> register (address h3E). |

**Register 4Fh. ADC8 Control**

| Bit  | D7            | D6 | D5        | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|-----------|----|----|----|----|----|
| Name | Reserved[7:6] |    | adc8[5:0] |    |    |    |    |    |
| Type | R/W           |    | R/W       |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                  |
|-----|-----------|---------------------------|
| 7:6 | Reserved  | <b>Reserved.</b>          |
| 5:0 | adc8[5:0] | <b>ADC8 Control Bits.</b> |

**Register 50h. Analog Test Bus Select**

| Bit  | D7       | D6 | D5 | D4       | D3 | D2 | D1 | D0 |
|------|----------|----|----|----------|----|----|----|----|
| Name | Reserved |    |    | atb[4:0] |    |    |    |    |
| Type | R/W      |    |    | R/W      |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function                                                                                                    |
|-----|----------|-------------------------------------------------------------------------------------------------------------|
| 7:5 | Reserved | <b>Reserved.</b>                                                                                            |
| 4:0 | atb[4:0] | <b>Analog Test Bus.</b><br>The selection of internal analog testpoints that are muxed onto TESTp and TESTn. |

Table 33. Internal Analog Signals Available on the Analog Test Bus

| atb[4:0] | GPIOx        | GPIOx        |
|----------|--------------|--------------|
| 1        | MixIp        | MixIn        |
| 2        | MixQp        | MixQn        |
| 3        | PGA_Ip       | PGA_In       |
| 4        | PGA_QP       | PGA_Qn       |
| 5        | ADC_vcm      | ADC_vcmb     |
| 6        | ADC_ipoly10u | ADC_ref      |
| 7        | ADC_Refdac_p | ADC_Refdac_n |
| 8        | ADC_ipoly10  | ADC_ipoly10  |
| 9        | ADC_Res1Ip   | ADC_Res1In   |
| 10       | ADC_Res1Qp   | ADC_Res1Qn   |
| 11       | Reserved     | Reserved     |
| 12       | Reserved     | Reserved     |
| 13       | Reserved     | Reserved     |
| 14       | Reserved     | Reserved     |
| 15       | Reserved     | Reserved     |
| 16       | Reserved     | Reserved     |
| 17       | Reserved     | Reserved     |
| 18       | ICP_Test     | PLL_IBG_05   |
| 19       | PLL_VBG      | VSS_VCO      |
| 20       | Vctrl_Test   | PLL_IPTAT_05 |
| 21       | PA_vbias     | Reserved     |
| 22       | DIGBG        | DIGVFB       |
| 23       | IFBG         | IFVFB        |
| 24       | PLLBG        | PLLVReg      |
| 25       | IBias10u     | IBias5u      |
| 26       | 32KRC_Ucap   | 32KRC_Ures   |
| 27       | ADC8_VIN     | ADC8_VDAC    |
| 28       | LBDcomp      | LBDcompref   |
| 29       | TSBG         | TSVtemp      |
| 30       | RFBG         | RFVREG       |
| 31       | VCOBG        | VCOVREG      |

**Register 51h. Digital Test Bus Select**

| Bit         | D7       | D6       | D5       | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----|----|----|----|----|
| <b>Name</b> | Reserved | ensctest | dtb[5:0] |    |    |    |    |    |
| <b>Type</b> | R/W      | R/W      | R/W      |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function                                                                        |
|-----|----------|---------------------------------------------------------------------------------|
| 7   | Reserved | <b>Reserved.</b>                                                                |
| 6   | ensctest | <b>Scan Test Enable.</b><br>When set to 1 then GPIO0 will be the ScanEn input.  |
| 5:0 | dtb[5:0] | <b>Digital Test Bus.</b><br>GPIO must be configured to Digital Test Mux output. |

**Table 34. Internal Digital Signals Available on the Digital Test Bus**

| dtb[4:0] | GPIO0           | Signal                         | GPIO1              | Signal                         | GPIO2           | Signal                        |
|----------|-----------------|--------------------------------|--------------------|--------------------------------|-----------------|-------------------------------|
| 0        | wkup_clk_32k    | wake-up 32kHz clock            | rbase_en           | first divided clock            | clk_base        | timebase clock                |
| 1        | wkup_clk_32k    | wake-up 32kHz clock            | wake_up            | wake-up event                  | tm1sec          | 1 sec timebase                |
| 2        | ts_adc_en       | aux. ADC enable                | adc_rdy_n          | aux. ADC conversion ready      | adc_done        | aux. ADC measurement done     |
| 3        | cont_lbd        | low battery continuous mode    | lbd_on             | low battery ON signal          | lbd             | unfiltered output of LBD      |
| 4        | div_clk_g       | gated divided clock            | uc_clk             | microcontroller clock          | ckout_rcsel     | slow clock selected           |
| 5        | en_div_sync     | clock divider enable (sync'ed) | en_ckout           | clock out enable               | en_ckout_s      | clock out enable (sync'ed)    |
| 6        | osc30_en        | oscillator enable              | osc30_bias2x       | oscillator bias control        | xok             | chip ready                    |
| 7        | xok             | chip ready                     | zero_cap           | cap. load zero                 | osc30_buff_en   | buffer enable                 |
| 8        | tsadc_needed    | aux. ADC enable                | ext_retran         | ext. retransmission request    | tx_mod_gpio     | TX modulation input           |
| 9        | gpio_0_oen_n    | GPIO0 output enable            | gpio_0_aen         | GPIO0 analog selection         | gpio_0_aden     | GPIO0 ADC input line enable   |
| 10       | int_ack1        | interrupt acknowledge 1        | int_ack2           | interrupt acknowledge 2        | int_store       | interrupt latch closed        |
| 11       | ext_int2        | ext. interrupt from GPIO2      | irq_bit8           | combined external status       | msk_bit8        | combined masked ext. int.     |
| 12       | sdo_aux_sel     | SDO aux. function select       | sdo_aux            | SDO aux. signal                | nirq_aux_sel    | nIRQ aux. function select     |
| 13       | trdata_on_sdi   | TX/RX data on SDI              | tx_mod             | TX modulation input            | tx_clk_out      | TX clock output               |
| 14       | start_full_sync | RC osc. full calibration start | start_fine_sync    | RC osc. fine calibration start | xtal_req        | crystal req. for RC osc. cal. |
| 15       | coarse_rdy      | RC osc. coarse cal. ready      | fine_rdy           | RC osc. fine cal. ready        | xtal_req_sync   | sync'ed crystal request       |
| 16       | vco_cal_rst_s_n | VCO calibration reset          | vco_cal            | VCO calibration is running     | vco_cal_done    | VCO calibration done          |
| 17       | vco_cal_en      | VCO calibration enable         | en_ref_cnt         | reference counter enable       | en_freq_cnt_s   | frequency counter enable      |
| 18       | vco_cal_en      | VCO calibration enable         | pos_diff           | positive difference to goal    | en_freq_cnt_s   | frequency counter enable      |
| 19       | dsm_clk_mux     | DSM multiplexed clock          | pll_fb_clk_tst     | PLL feedback clock             | pll_ref_clk_tst | PLL reference clock           |
| 20       | dsm[0]          | delta-sigma output             | dsm[1]             | delta-sigma output             | dsm[2]          | delta-sigma output            |
| 21       | dsm[3]          | delta-sigma output             | pll_fbdiv15        |                                | dsm_rst_s_n     | delta-sigma reset             |
| 22       | pll_en          | PLL enable: TUNE state         | pllt0_ok           | PLL initial settling OK        | pllts_ok        | PLL soft settling OK          |
| 23       | ch_freq_req     | frequency change request       | pllts_ok           | PLL soft settling OK           | vco_cal_done    | VCO calibration done          |
| 24       | vco_cal_en      | VCO calibration enable         | pll_vbias_shunt_en | VCO bias shunt enable          | prog_req        | frequency recalculation req.  |
| 25       | bandgap_en      | bandgap enable                 | frac_div_en        | fractional divider enable      | buff3_en        | buffer3 enable                |
| 26       | pll_pfd_up      | PFD up signal                  | pll_pfd_down       | PFD down signal                | pfd_up_down     | PFD output change (XOR'ed)    |
| 27       | pll_lock_detect | PLL lock detect                | pll_en             | PLL enable: TUNE state         | pllt0_ok        | PLL initial settling OK       |
| 28       | pll_en          | PLL enable: TUNE state         | pll_lock_detect    | PLL lock detect                | pllts_ok        | PLL soft settling OK          |
| 29       | pwst[0]         | internal power state           | pwst[1]            | internal power state           | pwst[2]         | internal power state          |

Table 34. Internal Digital Signals Available on the Digital Test Bus (Continued)

| dtb[4:0] | GPIO0          | Signal                       | GPIO1            | Signal                       | GPIO2                   | Signal                       |
|----------|----------------|------------------------------|------------------|------------------------------|-------------------------|------------------------------|
| 30       | xok            | chip ready: READY state      | pll_en           | PLL enable: TUNE state       | tx_en                   | TX enable: TX state          |
| 31       | ts_en          | temperature sensor enable    | auto_tx_on       | automatic TX ON              | tx_off                  | TX OFF                       |
| 32       | ch_freq_req    | frequency change request     | return_tx        | return from TX               | pk_sent                 | packet sent                  |
| 33       | retran_req     | retransmission request       | tx_ffpt_store    | TX FIFO pointer store        | tx_ffpt_restore         | TX FIFO pointer restore      |
| 34       | pa_on_trig     | PA ON trigger                | dly_5us_ok       | 5 us delay expired           | mod_dly_ok              | modulator delay expired      |
| 35       | tx_shdwn       | TX shutdown                  | ramp_start       | modulator ramp down start    | ramp_done               | modulator ramp down ended    |
| 36       | pk_sent_dly    | delayed packet sent          | tx_shdwn_done    | TX shutdown done             | pa_ramp_en              | PA ramp enable               |
| 37       | tx_en          | TX enable: TX state          | ldo_rf_precharge | RF LDO precharge             | pa_ramp_en              | PA ramp enable               |
| 38       | pa_on_trig     | TX enable: TX state          | dp_tx_en         | packet handler (TX) enable   | mod_en                  | modulator enable             |
| 39       | reg_wr_en      | register write enable        | reg_rd_en        | register rread enable        | addr_inc                | register address increment   |
| 40       | dp_tx_en       | packet handler (TX) enable   | data_start       | start of TX data             | pk_sent                 | packet has been sent         |
| 41       | data_start     | start of TX data             | tx_out           | packet handler TX data out   | pk_sent                 | packet has been sent         |
| 42       | ramp_done      | ramp is done                 | data_start       | start of TX data             | pk_tx                   | packet is being transmitted  |
| 43       | tx_ffaf        | TX FIFO almost full          | tx_fifo_wr_en    | TX FIFO write enable         | tx_ffem_tst             | internal TX FIFO empty       |
| 44       | clk_mod        | modulator gated 10MHz clock  | tx_clk           | TX clock from NCO            | rd_clk_x8               | read clock = tx_clk / 10     |
| 45       | mod_en         | modulator enable             | ramp_start       | start modulator ramping down | ramp_done               | modulator ramp done          |
| 46       | data_start     | data input start from PH     | ook_en           | OOK modulation enable        | ook (also internal PN9) | OOK modulation               |
| 47       | prog_req       | freq. channel update request | freq_err         | wrong freq. indication       | dsm_rst_s_n             | dsm sync. reset              |
| 48       | mod_en         | modulator enable             | tx_rdy           | TX ready                     | tx_clk                  | TX clock from NCO            |
| 49       | dp_rx_en       | packet handler (RX) enable   | prea_valid       | valid preamble               | pk_srch                 | packet is being searched     |
| 50       | pk_srch        | packet is being searched     | sync_ok          | sync. word has been detected | rx_data                 | packet handler RX data input |
| 51       | pk_rx          | packet is being received     | sync_ok          | sync. word has been detected | pk_valid                | valid packet received        |
| 52       | sync_ok        | sync. word has been detected | crc_error        | CRC error has been detected  | hdch_error              | header error detected        |
| 53       | direct_mode    | direct mode                  | rx_ffaf          | RX FIFO almost full          | rx_fifo_rd_en           | RX FIFO read enable          |
| 54       | bit_clk        | bit clock                    | prea_valid       | valid preamble               | rx_data                 | demodulator RX data output   |
| 55       | prea_valid     | valid preamble               | prea_inval       | invalid preamble             | ant_div_sw              | antenna switch (algorithm)   |
| 56       | sync_ok        | sync. word has been detected | bit_clk          | bit clock                    | rx_data                 | demodulator RX data output   |
| 57       | demod phase[4] | demodulator phase MSB        | demod phase [3]  | demodulator MSB-1            | demod phase [2]         | demodulator MSB-2            |
| 58       | prea_valid     | valid preamble               | demod_tst[2]     | demodulator test             | demod_tst[1]            | demodulator test             |
| 59       | agc_smp_clk    | AGC sample clock             | win_h_tp         | window comparator high       | win_l_tp                | window comparator low dly'd  |
| 60       | agc_smp_clk    | AGC sample clock             | win_h_dly_tp     | window comparator high       | win_l_dly_tp            | window comparator low dly'd  |
| 61       | ldc_on         | active low duty cycle        | pll_en           | PLL enable: TUNE state       | rx_en                   | RX enable: RX state          |
| 62       | ldc_on         | active low duty cycle        | no_sync_det      | no sync word detected        | prea_valid              | valid preamble               |
| 63       | adc_en         | ADC enable                   | adc_refdac_en    | ADC reference DAC enable     | adc_rst_n               | combined ADC reset           |

## Register 52h. TX Ramp Control

| Bit  | D7       | D6         | D5 | D4 | D3           | D2 | D1          | D0 |
|------|----------|------------|----|----|--------------|----|-------------|----|
| Name | Reserved | txmod[2:0] |    |    | ldoramp[1:0] |    | txramp[1:0] |    |
| Type | R/W      | R/W        |    |    | R/W          |    | R/W         |    |

Reset value = 00101111

| Bit | Name         | Function                                                                                                                                                                                                                            |
|-----|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved     | <b>Reserved</b>                                                                                                                                                                                                                     |
| 6:4 | txmod[2:0]   | <b>TX Modulation Delay.</b><br>The time delay between PA enable and the beginning of the TX modulation to allow for PA ramp-up. It can be set from 0 $\mu$ s to 28 $\mu$ s in 4 $\mu$ s steps. This also works during PA ramp down. |
| 3:2 | ldoramp[1:0] | <b>TX LDO Ramp Time.</b><br>The RF LDO is used to help ramp the PA to prevent VCO pulling and spectral splatter.<br>00: 5 $\mu$ s<br>01: 10 $\mu$ s<br>10: 15 $\mu$ s<br>11: 20 $\mu$ s                                             |
| 1:0 | txramp[1:0]  | <b>TX Ramp Time.</b><br>The PA is ramped up slowly to prevent VCO pulling and spectral splatter. This register sets the time the PA is ramped up.<br>00: 5 $\mu$ s<br>01: 10 $\mu$ s<br>10: 15 $\mu$ s<br>11: 20 $\mu$ s            |

The total settling time (cold start) of the PLL after the calibration can be calculated as  $T_{CS} = T_S + T_O$ .

## Register 53h. PLL Tune Time

| Bit  | D7         | D6 | D5 | D4 | D3 | D2    | D1 | D0 |
|------|------------|----|----|----|----|-------|----|----|
| Name | pllts[4:0] |    |    |    |    | pllt0 |    |    |
| Type | R/W        |    |    |    |    | R/W   |    |    |

Reset value = 01010010

| Bit | Name       | Function                                                                                                                                                                                                                                                                                                          |
|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | pllts[4:0] | <b>PLL Soft Settling Time (<math>T_S</math>).</b><br>This register will set the settling time for the PLL from a previous locked frequency in Tune mode. The value is configurable between 0 $\mu$ s and 310 $\mu$ s, in 10 $\mu$ s intervals. The default plltime corresponds to 100 $\mu$ s. See formula above. |
| 2:0 | pllt0      | <b>PLL Settling Time (<math>T_O</math>).</b><br>This register will set the time allowed for PLL settling after the calibrations are completed. The value is configurable between 0 $\mu$ s and 70 $\mu$ s, in 10 $\mu$ s steps. The default pllt0 corresponds to 20 $\mu$ s. See formula above.                   |

## Register 54h. PA Boost

| Bit  | D7            | D6 | D5         | D4 | D3 | D2           | D1 | D0             |
|------|---------------|----|------------|----|----|--------------|----|----------------|
| Name | Reserved[7:6] |    | inv_pre_th |    |    | ldo_pa_boost |    | pa_vbias_boost |
| Type | R/W           |    | R/W        |    |    | R/W          |    | R/W            |

Reset value = 01010100

| Bit | Name            | Function                           |
|-----|-----------------|------------------------------------|
| 7:6 | Reserved[7:6]   | <b>Reserved.</b>                   |
| 5:2 | inv_pre_th[5:2] | <b>Invalid Preamble Threshold.</b> |
| 1   | ldo_pa_boost    | <b>LDO PA Boost.</b>               |
| 0   | pa_vbias_boost  | <b>PA VBIAS Boost.</b>             |

Invalid preamble will be evaluated during this period: (invalid\_preamble\_Threshold x 4) x Bit Rate period.

**Register 55h. Calibration Control**

| Bit  | D7       | D6            | D5         | D4       | D3    | D2       | D1     | D0      |
|------|----------|---------------|------------|----------|-------|----------|--------|---------|
| Name | Reserved | xtalstarthalf | adccaldone | enrcfcal | rccal | vcocaldp | vcocal | skipvco |
| Type | R        | R/W           | R          | R/W      | R/W   | R/W      | R/W    | R/W     |

Reset value = x1x00100

| Bit | Name          | Function                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved      | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6   | xtalstarthalf | <b>If Set, the Xtal Wake Time Period is Halved.</b>                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5   | adccaldone    | <b>Delta-sigma ADC Calibration Done.</b> Reading this bit gives 1 if the calibration process has been finished.                                                                                                                                                                                                                                                                                                                                       |
| 4   | enrcfcal      | <b>RC Oscillator Fine Calibration Enable.</b><br>If this bit is set to 1 then the RC oscillator performs fine calibration in every app. 30 s.                                                                                                                                                                                                                                                                                                         |
| 3   | rccal         | <b>RC Calibration Force.</b><br>If setting rccal = 1 will automatically perform a forced calibration of the 32 kHz RC Oscillator. The RC OSC will automatically be calibrated if the Wake-Up-Timer is enabled or if in the Wake-on-Receiver state. The calibration takes 2 ms. The 32 kHz RC oscillator must be enabled to perform a calibration. Setting this signal from a 0 to 1 will initiate the calibration. This bit is cleared automatically. |
| 2   | vcocaldp      | <b>VCO Calibration Double Precision Enable.</b><br>When this bit is set to 1 then the VCO calibration measures longer thus calibrates more precisely.                                                                                                                                                                                                                                                                                                 |
| 1   | vcocal        | <b>VCO Calibration Force.</b><br>If in Idle Mode and pllcn = 1, setting vcocal = 1 will force a one time calibration of the synthesizer VCO. This bit is cleared automatically.                                                                                                                                                                                                                                                                       |
| 0   | skipvco       | <b>Skip VCO Calibration.</b><br>Setting skipvco = 1 will skip the VCO calibration when going from the Idle state to the TX or RX state.                                                                                                                                                                                                                                                                                                               |

## Register 56h. Modem Test

| Bit  | D7      | D6       | D5     | D4       | D3    | D2         | D1        | D0      |
|------|---------|----------|--------|----------|-------|------------|-----------|---------|
| Name | bcrfbyp | slicfbyp | dttype | oscdeten | ookth | refclkssel | refclkinv | distogg |
| Type | R/W     | R/W      | R/W    | R/W      | R/W   | R/W        | R/W       | R/W     |

Reset value = 00000000

| Bit | Name       | Function                                                                                                                                                          |
|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | bcrfbyp    | If set, BCR phase compensation will be bypassed.                                                                                                                  |
| 6   | slicfbyp   | If set, slicer phase compensation will be bypassed.                                                                                                               |
| 5   | dttype     | <b>Dithering Type.</b><br>If low and dither enabled, we add +1/0, otherwise if high and dithering enabled, we add $\pm 1$ .                                       |
| 4   | oscdeten   | If low, the ADC Oscillation Detection mechanism is allowed to work. If set, we disable the function.                                                              |
| 3   | ookth      | If set, in OOK mode, the slicer threshold will be estimated by 8 bits of preamble. By default, this bit is low and the demod estimate the threshold after 4 bits. |
| 2   | refclkssel | <b>Delta-Sigma Reference Clock Source Selection</b><br>1: 10 MHz<br>0: PLL                                                                                        |
| 1   | refclkinv  | <b>Delta-Sigma Reference Clock Inversion Enable.</b>                                                                                                              |
| 0   | distogg    | If reset, the discriminator toggling is disabled.                                                                                                                 |

## Register 57h. Charge Pump Test

| Bit  | D7     | D6        | D5        | D4        | D3     | D2          | D1 | D0 |
|------|--------|-----------|-----------|-----------|--------|-------------|----|----|
| Name | pfdrst | fbdiv_rst | cpforceup | cpforcedn | cdonly | cdcurr[2:0] |    |    |
| Type | R/W    | R/W       | R/W       | R/W       | R/W    | R/W         |    |    |

Reset value = 00000000

| Bit | Name        | Function                                 |
|-----|-------------|------------------------------------------|
| 7   | pfdrst      | <b>Direct Control to Analog.</b>         |
| 6   | fbdiv_rst   | <b>Direct Control to Analog.</b>         |
| 5   | cpforceup   | <b>Charge Pump Force Up.</b>             |
| 4   | cpforcedn   | <b>Charge Pump Force Down.</b>           |
| 3   | cdonly      | <b>Charge Pump DC Offset Only.</b>       |
| 2:0 | cdcurr[2:0] | <b>Charge Pump DC Current Selection.</b> |

**Register 58h. Charge Pump Current Trimming/Override**

| Bit         | D7          | D6 | D5       | D4         | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----------|------------|----|----|----|----|
| <b>Name</b> | cpcurr[1:0] |    | cpcorrov | cporr[4:0] |    |    |    |    |
| <b>Type</b> | R/W         |    | R/W      | R/W        |    |    |    |    |

Reset value = 100xxxxx

| Bit | Name        | Function                                                                                                                                                                                                                                           |
|-----|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | cpcurr[1:0] | <b>Charge Pump Current (Gain Setting).</b><br>Changing these bits will change the BW of the PLL. The default setting is adequate for all data rates.                                                                                               |
| 5   | cpcorrov    | <b>Charge Pump Correction Override Enable.</b>                                                                                                                                                                                                     |
| 4:0 | cpcorr[4:0] | <b>Charge Pump Correction Value.</b><br>During read, you read what the Charge Pump sees. If cpcorrov = 1, then the value you write will go to the Charge Pump, and will also be the value you read. By default, cpcorr[4:0] wakes up as all Zeros. |

**Register 59h. Divider Current Trimming/Delta-Sigma Test**

| Bit         | D7           | D6      | D5          | D4 | D3          | D2 | D1            | D0 |
|-------------|--------------|---------|-------------|----|-------------|----|---------------|----|
| <b>Name</b> | txcorboosten | fbdivhc | d3trim[1:0] |    | d2trim[1:0] |    | d1p5trim[1:0] |    |
| <b>Type</b> | R/W          | R/W     | R/W         |    | R/W         |    | R/W           |    |

Reset value = 10000000

| Bit | Name          | Function                                                                                            |
|-----|---------------|-----------------------------------------------------------------------------------------------------|
| 7   | txcorboosten  | <b>If this is Set, then vcocorr (reg 5A[5:2]) = 1111 during TX Mode and VCO CAL followed by TX.</b> |
| 6   | fbdivhc       | <b>Feedback (fractional) Divider High Current Enable (+5 <math>\mu</math>A).</b>                    |
| 5:4 | d3trim[1:0]   | <b>Divider 3 Current Trim Value.</b>                                                                |
| 3:2 | d2trim[1:0]   | <b>Divider 2 Current Trim Value.</b>                                                                |
| 1:0 | d1p5trim[1:0] | <b>Divider 1.5 (div-by-1.5) Current Trim Value.</b>                                                 |

## Register 5Ah. VCO Current Trimming

| Bit  | D7           | D6        | D5           | D4 | D3 | D2 | D1          | D0 |
|------|--------------|-----------|--------------|----|----|----|-------------|----|
| Name | txcurboosten | vcocorrov | vcocorr[3:0] |    |    |    | vcocur[1:0] |    |
| Type | R/W          | R/W       | R/W          |    |    |    | R/W         |    |

Reset value = 00000011

| Bit | Name         | Function                                                                    |
|-----|--------------|-----------------------------------------------------------------------------|
| 7   | txcurboosten | If this is Set, then vcocur = 11 during TX Mode and VCO CAL followed by TX. |
| 6   | vcocorrov    | VCO Current Correction Override.                                            |
| 5:2 | vcocorr[3:0] | VCO Current Correction Value.                                               |
| 1:0 | vcocur[1:0]  | VCO Current Trim Value.                                                     |

## Register 5Bh. VCO Calibration/Override

| Bit  | D7              | D6          | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|-------------|----|----|----|----|----|----|
| Name | vcocalov/vcdone | vcocal[6:0] |    |    |    |    |    |    |
| Type | R/W             | R/W         |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name             | Function                                                                                                                                                                                                                                                                                                                               |
|-----|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | vco-calov/vcdone | <b>VCO Calibration Override/Done.</b><br>When vcocalov = 0 the internal VCO calibration results may be viewed by reading the vcocal register. When vcocalov = 1 the VCO results may be overridden externally through the SPI by writing to the vcocal register. Reading this bit gives 1 if the calibration process has been finished. |
| 6:0 | vcocal[6:0]      | <b>VCO Calibration Results.</b>                                                                                                                                                                                                                                                                                                        |

## Register 5Ch. Synthesizer Test

| Bit  | D7    | D6      | D5      | D4     | D3           | D2 | D1        | D0    |
|------|-------|---------|---------|--------|--------------|----|-----------|-------|
| Name | dsmdt | vcotype | enoloop | dsmmod | dsorder[1:0] |    | dsrstmode | dsrst |
| Type | R/W   | R       | R/W     | R/W    | R/W          |    | R/W       | R/W   |

Reset value = 0x001110

| Bit | Name         | Function                                                                                                           |
|-----|--------------|--------------------------------------------------------------------------------------------------------------------|
| 7   | dsmdt        | <b>Enable DSM Dithering.</b><br>If low, dithering is disabled.                                                     |
| 6   | vcotype      | <b>VCO Type.</b><br>0: basic, constant K<br>1: single varactor, changing K                                         |
| 5   | enoloop      | <b>Open Loop Mode Enable.</b>                                                                                      |
| 4   | dsmmod       | <b>Delta-Sigma Modulus.</b><br>0: 64 000<br>1: 65 536                                                              |
| 3:2 | dsorder[1:0] | <b>Delta-Sigma Order.</b><br>00: 0 order<br>01: 1 <sup>st</sup> order<br>10: 2 <sup>nd</sup> order<br>11: Mash 111 |
| 1   | dsrstmode    | <b>Delta-Sigma Reset Mode.</b>                                                                                     |
| 0   | dsrst        | <b>Delta-Sigma Reset.</b>                                                                                          |

## Register 5Dh. Block Enable Override 1

| Bit  | D7    | D6    | D5    | D4   | D3    | D2     | D1     | D0    |
|------|-------|-------|-------|------|-------|--------|--------|-------|
| Name | enmix | enina | enpga | enpa | enbf5 | endv32 | enbf12 | enmx2 |
| Type | R/W   | R/W   | R/W   | R/W  | R/W   | R/W    | R/W    | R/W   |

Reset value = 00000000

| Bit | Name   | Function                         |
|-----|--------|----------------------------------|
| 7   | enmix  | Mixer Enable Override.           |
| 6   | enlna  | LNA Enable Override.             |
| 5   | enpga  | PGA Enable Override.             |
| 4   | enpa   | Power Amplifier Enable Override. |
| 3   | enbf5  | Buffer 5 Enable Override.        |
| 2   | endv32 | Divider 3_2 Enable Override.     |
| 1   | enbf12 | Buffer 1_2 Enable Override.      |
| 0   | enmx2  | Multiplexer 2 Enable Override.   |

## Register 5Eh. Block Enable Override 2

| Bit  | D7   | D6     | D5    | D4    | D3    | D2     | D1    | D0       |
|------|------|--------|-------|-------|-------|--------|-------|----------|
| Name | ends | enldet | enmx3 | enbf4 | enbf3 | enbf11 | enbf2 | pllreset |
| Type | R/W  | R/W    | R/W   | R/W   | R/W   | R/W    | R/W   | R/W      |

Reset value = 01000000

| Bit | Name     | Function                                                         |
|-----|----------|------------------------------------------------------------------|
| 7   | ends     | Delta-Sigma Enable Override.                                     |
| 6   | enldet   | Lock Detect Enable.<br>(direct control, does not need override!) |
| 5   | enmx3    | Multiplexer 3 Enable Override.                                   |
| 4   | enbf4    | Buffer 4 Enable Override.                                        |
| 3   | enbf3    | Buffer 3 Enable Override.                                        |
| 2   | enbf11   | Buffer 1_1 Enable Override.                                      |
| 1   | enbf2    | Buffer 2 Enable Override.                                        |
| 0   | pllreset | PLL Reset Enable Override.                                       |

**Register 5Fh. Block Enable Override 3**

| Bit  | D7     | D6     | D5    | D4      | D3       | D2    | D1   | D0   |
|------|--------|--------|-------|---------|----------|-------|------|------|
| Name | enfrdv | endv31 | endv2 | endv1p5 | dvbshunt | envco | encp | enbg |
| Type | R/W    | R/W    | R/W   | R/W     | R/W      | R/W   | R/W  | R/W  |

Reset value = 00000000

| Bit | Name     | Function                                  |
|-----|----------|-------------------------------------------|
| 7   | enfrdv   | Fractional Divider Enable Override.       |
| 6   | endv31   | Divider 3_1 Enable Override.              |
| 5   | endv2    | Divider 2 Enable Override.                |
| 4   | endv1p5  | Divider 1.5 (div-by-1.5) Enable Override. |
| 3   | dvbshunt | VCO Bias Shunt Enable Override Mode.      |
| 2   | envco    | VCO Enable Override.                      |
| 1   | encp     | Charge Pump Enable Override.              |
| 0   | enbg     | Bandgap Enable Override.                  |

**Register 60h. Channel Filter Coefficient Address**

| Bit  | D7       | D6 | D5 | D4 | D3            | D2 | D1 | D0 |
|------|----------|----|----|----|---------------|----|----|----|
| Name | Reserved |    |    |    | chfiladd[3:0] |    |    |    |
| Type | R/W      |    |    |    | R/W           |    |    |    |

Reset value = 00000000

| Bit | Name          | Function                                                                                                              |
|-----|---------------|-----------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved      | Reserved.                                                                                                             |
| 3:0 | chfiladd[3:0] | Channel Filter Coefficient Look-up Table Address.<br>The address for channel filter coefficients used in the RX path. |

**Register 61h. Channel Filter Coefficient Value**

| Bit         | D7       | D6 | D5            | D4 | D3  | D2 | D1 | D0 |
|-------------|----------|----|---------------|----|-----|----|----|----|
| <b>Name</b> | Reserved |    | chfilval[5:0] |    |     |    |    |    |
| <b>Type</b> | R/W      |    |               |    | R/W |    |    |    |

Reset value = 00000000

| Bit | Name          | Function                                                                             |
|-----|---------------|--------------------------------------------------------------------------------------|
| 7:6 | Reserved      | <b>Reserved.</b>                                                                     |
| 5:0 | chfilval[5:0] | <b>Filter Coefficient Value in the Look-up Table Addressed by the chfiladd[3:0].</b> |

**Register 62h. Crystal Oscillator/Power-on-Reset Control**

| Bit         | D7        | D6 | D5 | D4      | D3       | D2      | D1     | D0    |
|-------------|-----------|----|----|---------|----------|---------|--------|-------|
| <b>Name</b> | pwst[2:0] |    |    | clkhyst | enbias2x | enamp2x | bufovr | enbuf |
| <b>Type</b> | R         |    |    | R/W     | R/W      | R/W     | R/W    | R/W   |

Reset value = xxx00100

| Bit | Name      | Function                                                                                                                                                                                                        |
|-----|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | pwst[2:0] | <b>Internal Power States of the Chip.</b><br>LP: 000<br>RDY: 001<br>Tune: 011<br>TX: 010<br>RX: 111                                                                                                             |
| 4   | clkhyst   | <b>Clock Hysteresis Setting.</b>                                                                                                                                                                                |
| 3   | enbias2x  | <b>2 Times Higher Bias Current Enable.</b>                                                                                                                                                                      |
| 2   | enamp2x   | <b>2 Times Higher Amplification Enable.</b>                                                                                                                                                                     |
| 1   | bufovr    | <b>Output Buffer Enable Override.</b><br>If set to 1 then the enbuf bit controls the output buffer.<br>0: output buffer is controlled by the state machine.<br>1: output buffer is controlled by the enbuf bit. |
| 0   | enbuf     | <b>Output Buffer Enable.</b><br>This bit is active only if the bufovr bit is set to 1.                                                                                                                          |

**Register 63h. RC Oscillator Coarse Calibration/Override**

| Bit         | D7    | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|----------|----|----|----|----|----|----|
| <b>Name</b> | rccov | rcc[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/W   | R/W      |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function                                                                                                                                                                                                                                                                  |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | rccov    | <b>RC Oscillator Coarse Calibration Override.</b><br>When rccov = 0 the internal Coarse Calibration results may be viewed by reading the rccal register. When rccov = 1 the Coarse results may be overridden externally through the SPI by writing to the rccal register. |
| 6:0 | rcc[6:0] | <b>RC Oscillator Coarse Calibration Override Value/Results.</b>                                                                                                                                                                                                           |

**Register 64h. RC Oscillator Fine Calibration/Override**

| Bit         | D7    | D6       | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|----------|----|----|----|----|----|----|
| <b>Name</b> | rcfov | rcf[6:0] |    |    |    |    |    |    |
| <b>Type</b> | R/W   | R/W      |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function                                                                                                                                                                                                                                                              |
|-----|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | rcfov    | <b>RC Oscillator Fine Calibration Override.</b><br>When rcfov = 0 the internal Fine Calibration results may be viewed by reading the rcfcal register. When rcfov = 1 the Fine results may be overridden externally through the SPI by writing to the rcfcal register. |
| 6:0 | rcf[6:0] | <b>RC Oscillator Fine Calibration Override Value/Results.</b>                                                                                                                                                                                                         |

## Register 65h. LDO Control Override

| Bit  | D7     | D6     | D5       | D4      | D3     | D2      | D1       | D0       |
|------|--------|--------|----------|---------|--------|---------|----------|----------|
| Name | enspor | enbias | envcoldo | enifldo | enrldo | enplldo | endigldo | endigpwn |
| Type | R/W    | R/W    | R/W      | R/W     | R/W    | R/W     | R/W      | R/W      |

Reset value = 10000001

| Bit | Name     | Function                                            |
|-----|----------|-----------------------------------------------------|
| 7   | enspor   | Smart POR Enable.                                   |
| 6   | enbias   | Bias Enable.                                        |
| 5   | envcoldo | VCO LDO Enable.                                     |
| 4   | enifldo  | IF LDO Enable.                                      |
| 3   | enrldo   | RF LDO Enable.                                      |
| 2   | enplldo  | PLL LDO Enable.                                     |
| 1   | endigldo | Digital LDO Enable.                                 |
| 0   | endigpwn | Digital Power Domain Powerdown Enable in Idle Mode. |

## Register 66h. LDO Level Settings

| Bit  | D7    | D6     | D5   | D4     | D3       | D2 | D1     | D0 |
|------|-------|--------|------|--------|----------|----|--------|----|
| Name | enovr | enxtal | ents | enrc32 | Reserved |    | diglvl |    |
| Type | R/W   | R/W    | R/W  | R/W    | R        |    | R/W    |    |

Reset value = 00000011

| Bit | Name     | Function                                                                                                                                                    |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | enovr    | <b>Enable Overrides.</b><br>If high, ovr values are output to the blocks and can enable or disable them, if low, some ovr value can only enable the blocks. |
| 6   | enxtal   | Xtal Override Enable Value.                                                                                                                                 |
| 5   | ents     | Temperature Sensor Enable.                                                                                                                                  |
| 4   | enrc32   | 32K Oscillator Enable.                                                                                                                                      |
| 3   | Reserved | Reserved.                                                                                                                                                   |
| 2:0 | diglvl   | Digital LDO Level Setting.                                                                                                                                  |

**Register 67h. Delta-Sigma ADC Tuning 1**

| Bit  | D7     | D6       | D5    | D4         | D3           | D2 | D1 | D0 |
|------|--------|----------|-------|------------|--------------|----|----|----|
| Name | adcrst | enrefdac | enadc | adctuneovr | adctune[3:0] |    |    |    |
| Type | R/W    | R/W      | R/W   | R/W        | R/W          |    |    |    |

Reset value = 00011101

| Bit | Name         | Function                                        |
|-----|--------------|-------------------------------------------------|
| 7   | adcrst       | Delta-Sigma ADC Reset.                          |
| 6   | enrefdac     | Delta-Sigma ADC Reference DAC Enable Override.  |
| 5   | enadc        | Delta-Sigma ADC Enable Override.                |
| 4   | adctuneovr   | Resonator RC Calibration Value Override Enable. |
| 3:0 | adctune[3:0] | Resonator RC Calibration Value.                 |

**Register 68h. Delta-Sigma ADC Tuning 2**

| Bit  | D7       | D6 | D5 | D4    | D3       | D2          | D1 | D0 |
|------|----------|----|----|-------|----------|-------------|----|----|
| Name | Reserved |    |    | envcm | adcoloop | adcref[2:0] |    |    |
| Type | R        |    |    | R/W   | R/W      | R/W         |    |    |

Reset value = 00000011

| Bit | Name        | Function                                                                                          |
|-----|-------------|---------------------------------------------------------------------------------------------------|
| 7:5 | Reserved    | Reserved.                                                                                         |
| 4   | envcm       | Delta-Sigma ADC VCM Enable Override.                                                              |
| 3   | adcoloop    | Delta-Sigma ADC Open Loop Enable.                                                                 |
| 2:0 | adcref[2:0] | Delta-Sigma ADC Reference Voltage.<br>000: 0.5 V<br>001: 0.6 V<br>010: 0.7 V<br>...<br>111: 1.2 V |

## Register 69h. AGC Override 1

| Bit  | D7       | D6 | D5    | D4      | D3       | D2 | D1 | D0 |
|------|----------|----|-------|---------|----------|----|----|----|
| Name | Reserved |    | agcen | Inagain | pga[3:0] |    |    |    |
| Type | R        |    | R/W   | R/W     | R/W      |    |    |    |

Reset value = 00100000

| Bit | Name     | Function                                                                                                                                                                                                |
|-----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved | <b>Reserved.</b>                                                                                                                                                                                        |
| 5   | agcen    | <b>Automatic Gain Control Enable.</b><br>When this bit is set then the result of the control can be read out from bits [4:0], otherwise the gain can be controlled manually by writing into bits [4:0]. |
| 4   | Inagain  | <b>LNA Gain Select.</b><br>0 – min. gain = 5 dB      1 – max. gain = 25 dB                                                                                                                              |
| 3:0 | pga[3:0] | <b>PGA Gain Override Value.</b><br>000: 0 dB<br>001: 3 dB<br>010: 6 dB<br>...<br>101: 24 dB max.                                                                                                        |

## Register 6Ah. AGC Override 2

| Bit  | D7      | D6      | D5           | D4 | D3 | D2         | D1 | D0 |
|------|---------|---------|--------------|----|----|------------|----|----|
| Name | agcovpm | agcslow | Inacomp[3:0] |    |    | pgath[1:0] |    |    |
| Type | R/W     | R/W     | R/W          |    |    | R/W        |    |    |

Reset value = 10011101

| Bit | Name         | Function                                                                                                                                                                           |
|-----|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | agcovpm      | <b>If set, AGC will ignore the Preamble Detection.</b>                                                                                                                             |
| 6   | agcslow      | <b>AGC Slow Gain Increase Enable.</b><br>When this bit is set then the AGC loop will slow down the gain increase in the receiver. The speed of the gain reduction is not affected. |
| 5:2 | Inacomp[3:0] | <b>LNA Gain Compensation.</b><br>This bit is used for smoothing RSSI value when LNA gain is switched.                                                                              |
| 1:0 | pgath[1:0]   | <b>Window Comparator Reference Voltage Adjust in the PGA.</b>                                                                                                                      |

**Register 6Bh. GFSK FIR Filter Coefficient Address**

| Bit  | D7       | D6 | D5 | D4 | D3 | D2          | D1 | D0 |
|------|----------|----|----|----|----|-------------|----|----|
| Name | Reserved |    |    |    |    | firadd[2:0] |    |    |
| Type | R        |    |    |    |    | R/W         |    |    |

Reset value = xxxxx000

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | Reserved    | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2:0 | firadd[2:0] | <b>GFSK FIR Filter Coefficient Look-up Table Address.</b><br>The address for Gaussian filter coefficients used in the TX path. The default GFSK setting is for BT = 0.5. It is not needed to change or load the GFSK Coefficients if BT = 0.5 is satisfactory for the system.<br>000: i_coe0 (Default = d1)<br>001: i_coe1 (Default = d3)<br>010: i_coe2 (Default = d6)<br>011: i_coe3 (Default = d10)<br>100: i_coe4 (Default = d15)<br>101: i_coe5 (Default = d19)<br>110: i_coe6 (Default = d20) |

**Register 6Ch. GFSK FIR Filter Coefficient Value**

| Bit  | D7       | D6 | D5          | D4 | D3  | D2 | D1 | D0 |
|------|----------|----|-------------|----|-----|----|----|----|
| Name | Reserved |    | firval[5:0] |    |     |    |    |    |
| Type | R/W      |    |             |    | R/W |    |    |    |

Reset value = xxxxx000

| Bit | Name        | Function                                                                                                                            |
|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved    | <b>Reserved.</b>                                                                                                                    |
| 5:0 | firval[5:0] | <b>FIR Coefficient Value in the Look-up Table Addressed by the firadd[2:0].</b><br>The default coefficient can be read or modified. |

## Register 6Dh. TX Power

| Bit  | D7       | D6 | D5 | D4 | D3     | D2         | D1 | D0 |
|------|----------|----|----|----|--------|------------|----|----|
| Name | Reserved |    |    |    | lna_sw | txpow[2:0] |    |    |
| Type | R        |    |    |    | R/W    | R/W        |    |    |

Reset value = xxxx1000

| Bit | Name       | Function                                                                                                                                                                                     |
|-----|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved   | <b>Reserved.</b>                                                                                                                                                                             |
| 3   | lna_sw     | <b>LNA Switch Controller.</b><br>If set, lna_sw control from the digital will go high during TX modes, and low during other times. If reset, the digital control signal is low at all times. |
| 2:0 | txpow[2:0] | <b>TX Output Power.</b><br>The output power is configurable from –8 dBm to +13 dBm in ~3 dBm steps. txpow[2:0] = 111 corresponds to +13 dBm and 000 to –8 dBm.                               |

## Register 6Eh. TX Data Rate 1

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | txdr[15:8] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = 00001010

| Bit | Name       | Function                                           |
|-----|------------|----------------------------------------------------|
| 7:0 | txdr[15:8] | <b>Data Rate Upper Byte.</b><br>See formula above. |

The data rate can be calculated as:  $TX\_DR = 10^3 \times txdr[15:0] / 2^{16}$  [kbps] (if address 70[5] = 0) **or**

The data rate can be calculated as:  $TX\_DR = 10^3 \times txdr[15:0] / 2^{21}$  [kbps] (if address 70[5] = 1)

**Register 6Fh. TX Data Rate 0**

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | txdr[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00111101

| Bit | Name      | Function                                                               |
|-----|-----------|------------------------------------------------------------------------|
| 7:0 | txdr[7:0] | <b>Data Rate Lower Byte.</b><br>See formula above. Defaults = 40 kbps. |

**Register 70h. Modulation Mode Control 1**

| Bit  | D7       | D6 | D5          | D4       | D3      | D2       | D1      | D0      |
|------|----------|----|-------------|----------|---------|----------|---------|---------|
| Name | Reserved |    | txdtrtscale | enphpwdn | manppol | enmaninv | enmanch | enwhite |
| Type | R        |    | R/W         | R/W      | R/W     | R/W      | R/W     | R/W     |

Reset value = 00001100

| Bit | Name        | Function                                                                                                                                                                                                              |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | Reserved    | <b>Reserved.</b>                                                                                                                                                                                                      |
| 5   | txdtrtscale | <b>This bit should be set for Data Rates below 30 kbps.</b>                                                                                                                                                           |
| 4   | enphpwdn    | <b>If set, the Packet Handler will be powered down when chip is in low power mode.</b>                                                                                                                                |
| 3   | manppol     | <b>Manchester Preamble Polarity (will transmit a series of 1 if set, or series of 0 if reset).</b><br>This bit affects ONLY the transmitter side, not the receiver. This is valid ONLY if Manchester Mode is enabled. |
| 2   | enmaninv    | <b>Manchester Data Inversion is Enabled if this bit is set.</b>                                                                                                                                                       |
| 1   | enmanch     | <b>Manchester Coding is Enabled if this bit is set.</b>                                                                                                                                                               |
| 0   | enwhite     | <b>Data Whitening is Enabled if this bit is set.</b>                                                                                                                                                                  |

## Register 71h. Modulation Mode Control 2

| Bit  | D7         | D6 | D5         | D4 | D3    | D2    | D1          | D0 |
|------|------------|----|------------|----|-------|-------|-------------|----|
| Name | trclk[1:0] |    | dtmod[1:0] |    | eninv | fd[8] | modtyp[1:0] |    |
| Type | R/W        |    | R/W        |    | R/W   | R/W   | R/W         |    |

Reset value = 00000000

| Bit | Name        | Function                                                                                                                                                                                                                                                                                                                                  |
|-----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | trclk[1:0]  | <b>TX Data Clock Configuration.</b><br>00: No TX Data CLK is available (asynchronous mode – Can only work with modulations FSK or OOK).<br>01: TX Data CLK is available via the GPIO (one of the GPIO's should be programmed as well).<br>10: TX Data CLK is available via the SDO pin.<br>11: TX Data CLK is available via the nIRQ pin. |
| 5:4 | dtmod[1:0]  | <b>Modulation Source.</b><br>00: Direct Mode using TX_Data function via the GPIO pin (one of the GPIO's should be programmed accordingly as well)<br>01: Direct Mode using TX_Data function via the SDI pin (only when nSEL is high)<br>10: FIFO Mode<br>11: PN9 (internally generated)                                                   |
| 3   | eninv       | <b>Invert TX and RX Data.</b>                                                                                                                                                                                                                                                                                                             |
| 2   | fd[8]       | <b>MSB of Frequency Deviation Setting, see "Register 72h. Frequency Deviation".</b>                                                                                                                                                                                                                                                       |
| 1:0 | modtyp[1:0] | <b>Modulation Type.</b><br>00: Unmodulated carrier<br>01: OOK<br>10: FSK<br>11: GFSK (enable TX Data CLK (trclk[1:0]) when direct mode is used)                                                                                                                                                                                           |

The frequency deviation can be calculated:  $Fd = 625 \text{ Hz} \times fd[8:0]$ .

**Register 72h. Frequency Deviation**

| Bit  | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|----|----|----|----|----|----|----|
| Name | fd[7:0] |    |    |    |    |    |    |    |
| Type | R/W     |    |    |    |    |    |    |    |

Reset value = 00100000

| Bit | Name    | Function                                                  |
|-----|---------|-----------------------------------------------------------|
| 7:0 | fd[7:0] | <b>Frequency Deviation Setting.</b><br>See formula above. |

**Note:** It's recommended to use modulation index of 1 or higher (maximum allowable modulation index is 32). The modulation index is defined by  $2F_N/F_R$  where  $F_D$  is the deviation and  $R_B$  is the data rate. When Manchester coding is enabled the modulation index is defined by  $F_D/R_B$ .

**Register 73h. Frequency Offset 1**

| Bit  | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|----|----|----|----|----|----|----|
| Name | fo[7:0] |    |    |    |    |    |    |    |
| Type | R/W     |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name    | Function                                                                                                                                                                                                                                                                                                   |
|-----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | fo[7:0] | <b>Frequency Offset Setting.</b><br>The frequency offset can be calculated as $\text{Offset} = 156.25 \text{ Hz} \times (\text{hbssel} + 1) \times \text{fo}[7:0]$ .<br>fo[9:0] is a twos complement value. Reading from this register will give the AFC correction last results, not this register value. |

Reading from this register will give the AFC correction last results, not this register value.

## Register 74h. Frequency Offset 2

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1      | D0 |
|------|----------|----|----|----|----|----|---------|----|
| Name | Reserved |    |    |    |    |    | fo[9:8] |    |
| Type | R        |    |    |    |    |    | R/W     |    |

Reset value = 00000000

| Bit | Name     | Function                                                                                                                                                                                                                                                                                               |
|-----|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | Reserved | <b>Reserved.</b>                                                                                                                                                                                                                                                                                       |
| 1:0 | fo[9:8]  | <b>Upper Bits of the Frequency Offset Setting.</b><br>fo[9] is the sign bit. The frequency offset can be calculated as Offset = 156.25 Hz x (hbssel + 1) x fo[7:0]. fo[9:0] is a twos complement value. Reading from this register will give the AFC correction last results, not this register value. |

## Register 75h. Frequency Band Select

| Bit  | D7       | D6    | D5     | D4      | D3 | D2 | D1 | D0 |
|------|----------|-------|--------|---------|----|----|----|----|
| Name | Reserved | sbsel | hbssel | fb[4:0] |    |    |    |    |
| Type | R        | R/W   | R/W    | R/W     |    |    |    |    |

Reset value = 01110101

| Bit | Name     | Function                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | Reserved | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                              |
| 6   | sbsel    | <b>Side Band Select.</b>                                                                                                                                                                                                                                                                                                                                                      |
| 5   | hbssel   | <b>High Band Select.</b><br>Setting hbssel = 1 will choose the frequency range from 480–930 MHz (high bands). Setting hbssel = 0 will choose the frequency range from 240–479.9 MHz (low bands).                                                                                                                                                                              |
| 4:0 | fb[4:0]  | <b>Frequency Band Select.</b><br>Every increment corresponds to a 10 MHz Band for the Low Bands and a 20 MHz Band for the High Bands. Setting fb[4:0] = 00000 corresponds to the 240–250 MHz Band for hbssel = 0 and the 480–500 MHz Band for hbssel = 1. Setting fb[4:0] = 00001 corresponds to the 250–260 MHz Band for hbssel = 0 and the 500–520 MHz Band for hbssel = 1. |

The RF carrier frequency can be calculated as follows:

$$f_{\text{carrier}} = (f_b + 24 + (f_c + f_o) / 64000) \times 10000 \times (\text{hbssel} + 1) + (f_{\text{hch}} \times f_{\text{hs}} \times 10) \text{ [kHz]},$$

where parameters  $f_c$ ,  $f_o$ ,  $f_b$  and  $\text{hb\_sel}$  come from registers 73h–77h. Parameters  $f_{\text{hch}}$  and  $f_{\text{hs}}$  come from register 79h and 7Ah.

**Register 76h. Nominal Carrier Frequency**

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | fc[15:8] |    |    |    |    |    |    |    |
| Type | R/W      |    |    |    |    |    |    |    |

Reset value = 10111011

| Bit | Name     | Function                                                        |
|-----|----------|-----------------------------------------------------------------|
| 7:0 | fc[15:8] | <b>Nominal Carrier Frequency Setting.</b><br>See formula above. |

**Register 77h. Nominal Carrier Frequency**

| Bit  | D7      | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------|----|----|----|----|----|----|----|
| Name | fc[7:0] |    |    |    |    |    |    |    |
| Type | R/W     |    |    |    |    |    |    |    |

Reset value = 10000000

| Bit | Name    | Function                                                        |
|-----|---------|-----------------------------------------------------------------|
| 7:0 | fc[7:0] | <b>Nominal Carrier Frequency Setting.</b><br>See formula above. |

**Register 78h. Miscellaneous Settings**

| Bit  | D7            | D6 | D5 | D4 | D3         | D2             | D1 | D0 |
|------|---------------|----|----|----|------------|----------------|----|----|
| Name | Reserved[7:4] |    |    |    | Alt_PA_Seq | rcosc_cal[2:0] |    |    |
| Type | R/W           |    |    |    | R/W        | R/W            |    |    |

Reset value = 01111000

| Bit | Name           | Function                                                                                                                                                                                 |
|-----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Reserved[7:4]  | <b>Reserved.</b>                                                                                                                                                                         |
| 3   | Alt_PA_Seq     | <b>Alternative PA sequencing.</b><br>If set, we will enable the alternative PA sequence. By default, this is not enabled.                                                                |
| 2:0 | rcosc_cal[2:0] | <b>rcosc_cal[2:0].</b><br>Fine changes on the RC OSC Calibration target frequency, to help compensate for “calibration biases.” <b>This register should not be changed by costumers.</b> |

## Register 79h. Frequency Hopping Channel Select

| Bit  | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------|----|----|----|----|----|----|----|
| Name | fhch[7:0] |    |    |    |    |    |    |    |
| Type | R/W       |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name      | Function                          |
|-----|-----------|-----------------------------------|
| 7:0 | fhch[7:0] | Frequency Hopping Channel Number. |

## Register 7Ah. Frequency Hopping Step Size

| Bit  | D7       | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------|----|----|----|----|----|----|----|
| Name | fhs[7:0] |    |    |    |    |    |    |    |
| Type | R/W      |    |    |    |    |    |    |    |

Reset value = 00000000

| Bit | Name     | Function                                                                                                                                         |
|-----|----------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | fhs[7:0] | Frequency Hopping Step Size in 10 kHz Increments.<br>See formula for the nominal carrier frequency at "Register 76h. Nominal Carrier Frequency". |

**Register 7Bh. Turn Around and 15.4 Length Compliance**

| Bit         | D7          | D6            | D5 | D4 | D3 | D2             | D1         | D0 |
|-------------|-------------|---------------|----|----|----|----------------|------------|----|
| <b>Name</b> | 15.4 Length | Reserved[6:3] |    |    |    | turn_around_en | phase[1:0] |    |
| <b>Type</b> | R/W         | R/W           |    |    |    | R/W            | R/W        |    |

Reset value = 01111011

| Bit | Name           | Function                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | 15.4 Length    | <b>15.4 Packet Length Compliance.</b><br>If set, then PK Length definition for both TX and RX will also include the CRC bytes, If reset, then the Length refers ONLY to the DATA payload. For example, writing “9” to this register when it is set, means we are sending/expecting “7” bytes of DATA, and the other “2” should be the CRC (CRC should be enabled separately). |
| 6:3 | Reserved[6:3]  | <b>Reserved.</b>                                                                                                                                                                                                                                                                                                                                                              |
| 2   | turn_around_en | <b>Turn Around Enable.</b><br>Enabling for the turn around functionality.                                                                                                                                                                                                                                                                                                     |
| 1:0 | phase[1:0]     | <b>Turn Around Phase.</b><br>The RX to TX and vice-versa change in frequency will happen (if bit [2] is set) at the last byte, and these two registers set the bit position in which the frequency shifts should occur. Make sure it does not happen too early otherwise the last bits will be missed.                                                                        |

**Register 7Ch. TX FIFO Control 1**

| Bit         | D7       | D6 | D5           | D4 | D3  | D2 | D1 | D0 |
|-------------|----------|----|--------------|----|-----|----|----|----|
| <b>Name</b> | Reserved |    | txafthr[5:0] |    |     |    |    |    |
| <b>Type</b> | R/W      |    |              |    | R/W |    |    |    |

Reset value = 00110111

| Bit | Name         | Function                              |
|-----|--------------|---------------------------------------|
| 7:6 | Reserved     | <b>Reserved.</b>                      |
| 5:0 | txafthr[5:0] | <b>TX FIFO Almost Full Threshold.</b> |

## Register 7Dh. TX FIFO Control 2

| Bit  | D7       | D6 | D5            | D4 | D3  | D2 | D1 | D0 |
|------|----------|----|---------------|----|-----|----|----|----|
| Name | Reserved |    | txfaethr[5:0] |    |     |    |    |    |
| Type | R/W      |    |               |    | R/W |    |    |    |

Reset value = 00000100

| Bit | Name          | Function                        |
|-----|---------------|---------------------------------|
| 7:6 | Reserved      | Reserved.                       |
| 5:0 | txfaethr[5:0] | TX FIFO Almost Empty Threshold. |

## Register 7Eh. RX FIFO Control

| Bit  | D7       | D6 | D5           | D4 | D3  | D2 | D1 | D0 |
|------|----------|----|--------------|----|-----|----|----|----|
| Name | Reserved |    | rxafthr[5:0] |    |     |    |    |    |
| Type | R/W      |    |              |    | R/W |    |    |    |

Reset value = 00110111

| Bit | Name         | Function                       |
|-----|--------------|--------------------------------|
| 7:6 | Reserved     | Reserved.                      |
| 5:0 | rxafthr[5:0] | RX FIFO Almost Full Threshold. |

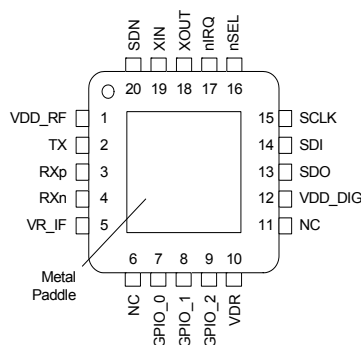
## Register 7Fh. FIFO Access

| Bit  | D7         | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------|----|----|----|----|----|----|----|
| Name | fifod[7:0] |    |    |    |    |    |    |    |
| Type | R/W        |    |    |    |    |    |    |    |

Reset value = NA

| Bit | Name       | Function                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | fifod[7:0] | <b>FIFO Data.</b><br>A Write (R/W = 1) to this Address will begin a Burst Write to the TX FIFO. The FIFO will be loaded in the same manner as a Burst SPI Write but the SPI address will not be incremented. To conclude the TX FIFO Write the SEL pin should be brought HIGH. A Read (R/W = 0) to this address will begin a burst read of the RX FIFO, in the same manner. |

### 13. Pin Descriptions: Si4431



| Pin | Pin Name   | I/O | Description                                                                                                                                                                                                                                                                                                                                                                             |
|-----|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | VDD_RF     | VDD | +1.8 to +3.6 V supply voltage input to all analog +1.7 V regulators. The recommended $V_{DD}$ supply voltage is +3.3 V.                                                                                                                                                                                                                                                                 |
| 2   | TX         | O   | Transmit output pin. The maximum level in TX mode is +13 dBm. The PA output is an open-drain connection so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.                                                                                                                                                                                                                |
| 3   | RXp        | I   | Differential RF input pins of the LNA. See application schematic for example matching network.                                                                                                                                                                                                                                                                                          |
| 4   | RXn        | I   |                                                                                                                                                                                                                                                                                                                                                                                         |
| 5   | VR_IF      | O   | Regulated Output Voltage of the IF 1.7 V Regulator. A 1 $\mu$ F decoupling capacitor is required.                                                                                                                                                                                                                                                                                       |
| 6   | NC         | —   | No Connect.                                                                                                                                                                                                                                                                                                                                                                             |
| 7   | GPIO_0     | I/O | General Purpose Digital I/O that may be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.                                                          |
| 8   | GPIO_1     | I/O |                                                                                                                                                                                                                                                                                                                                                                                         |
| 9   | GPIO_2     | I/O |                                                                                                                                                                                                                                                                                                                                                                                         |
| 10  | VDR        | O   | Regulated Output Voltage of the Digital 1.7 V Regulator. A 1 $\mu$ F decoupling capacitor is required.                                                                                                                                                                                                                                                                                  |
| 11  | NC         | —   | No Connect.                                                                                                                                                                                                                                                                                                                                                                             |
| 12  | VDD_DIG    | VDD | +1.8 to +3.6 V supply voltage input to the Digital +1.7 V Regulator. The recommended $V_{DD}$ supply voltage is +3.3 V.                                                                                                                                                                                                                                                                 |
| 13  | SDO        | O   | 0- $V_{DD}$ V digital output that provides a serial readback function of the internal control registers.                                                                                                                                                                                                                                                                                |
| 20  | SDI        | I   | Serial Data input. 0- $V_{DD}$ V digital input. This pin provides the serial data stream for the 4-line serial data bus.                                                                                                                                                                                                                                                                |
| 21  | SCLK       | I   | Serial Clock input. 0- $V_{DD}$ V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si4431 on positive edge transitions.                                                                                                                                                                                         |
| 22  | nSEL       | I   | Serial Interface Select input. 0- $V_{DD}$ V digital input. This pin provides the Select/Enable function for the 4-line serial data bus. The signal is also used to signify burst read/write mode.                                                                                                                                                                                      |
| 23  | nIRQ       | O   | General Microcontroller Interrupt Status output. When the Si4431 exhibits anyone of the Interrupt Events the nIRQ pin will be set low=0. Please see the Control Logic registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interrupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h. |
| 24  | XOUT       | O   | Crystal Oscillator Output. Connect to an external 30 MHz crystal or leave floating if driving the Xin pin with an external signal source.                                                                                                                                                                                                                                               |
| 25  | XIN        | I   | Crystal Oscillator Input. Connect to an external 30 MHz crystal or to an external source. If using an external clock source with no crystal, dc coupling with a nominal 0.8 VDC level is recommended with a minimum ac amplitude of 700 mVpp.                                                                                                                                           |
| 26  | SDN        | I   | Shutdown input pin. 0- $V_{DD}$ V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shutdown and the contents of the registers will be lost.                                                                                                                                                                                  |
| PKG | PADDLE_GND | GND | The exposed metal paddle on the bottom of the Si4431 supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the Si4431.                                                                                                                     |

## 14. Ordering Information

| Part Number*                                                                                                            | Description                | Package Type      | Operating Temperature |
|-------------------------------------------------------------------------------------------------------------------------|----------------------------|-------------------|-----------------------|
| Si4431-A0-FM                                                                                                            | ISM EZRadioPRO Transceiver | QFN-20<br>Pb-free | –40 to 85 °C          |
| <b>*Note:</b> Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel. |                            |                   |                       |



## CONTACT INFORMATION

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